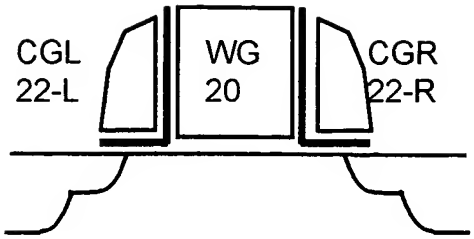


Fig. 1A

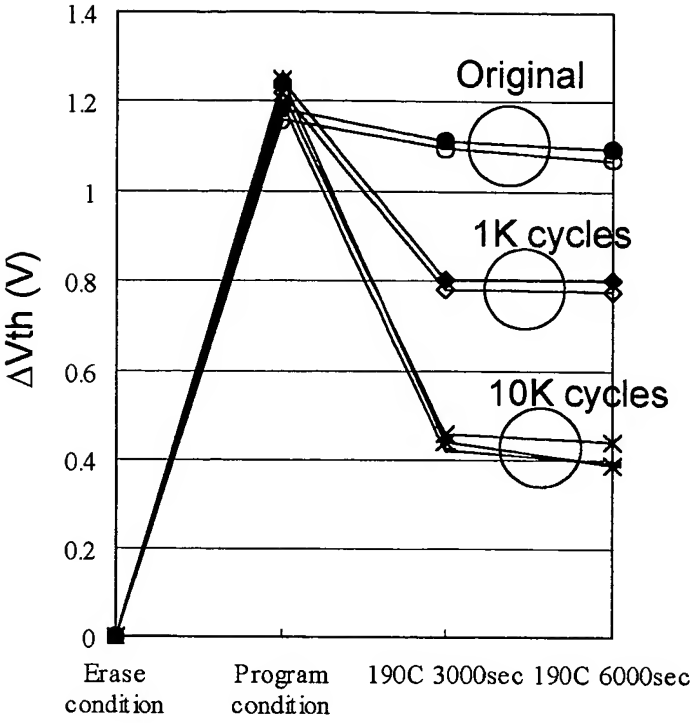


Fig. 1

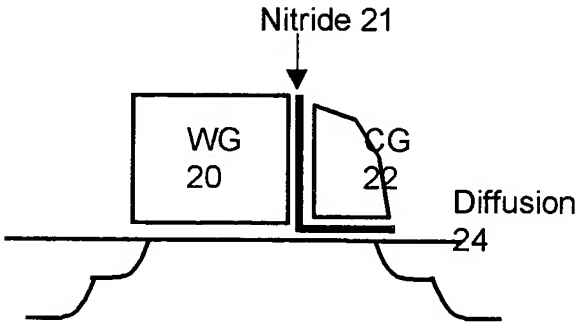


Fig.2

Prior Art

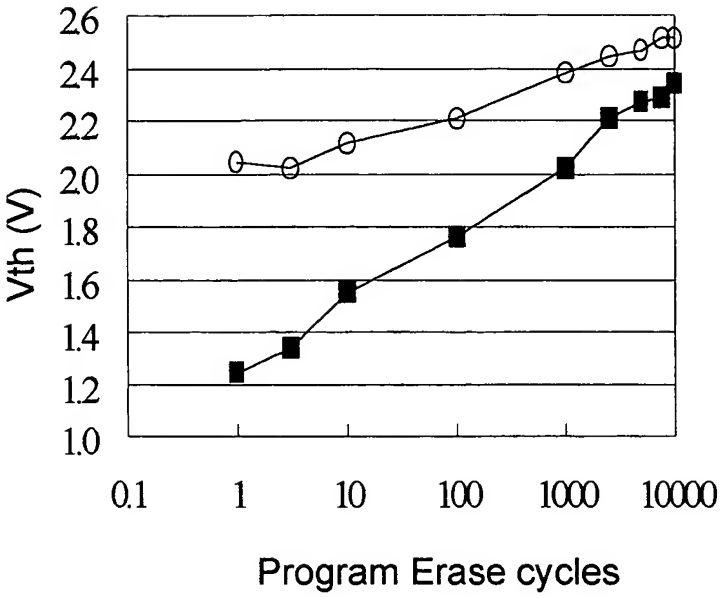

2.6
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
Vth (V)
0.1
1
10
100
1000
10000
Program Erase cycles

Fig.3

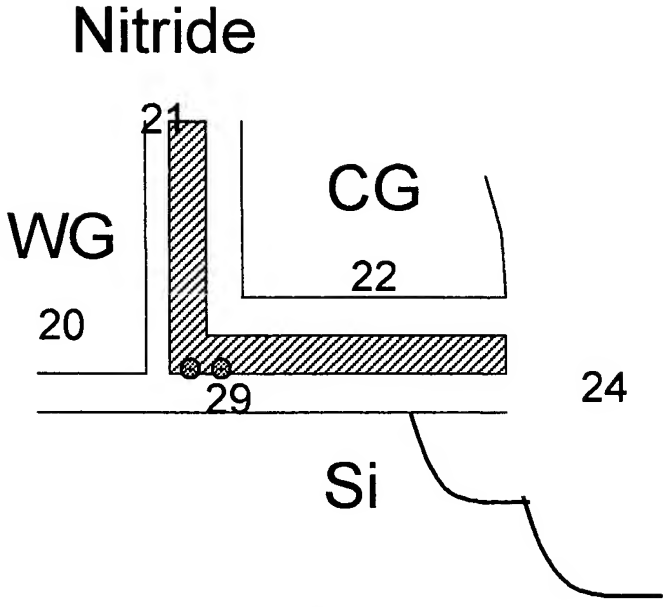

Nitride
21
CG
WG
22
20
29
24
Si

Fig.4

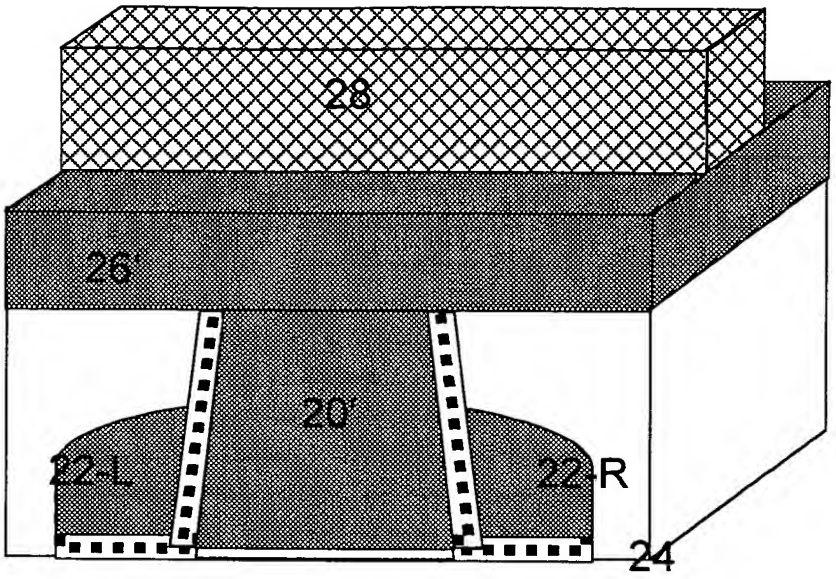


Fig.5A

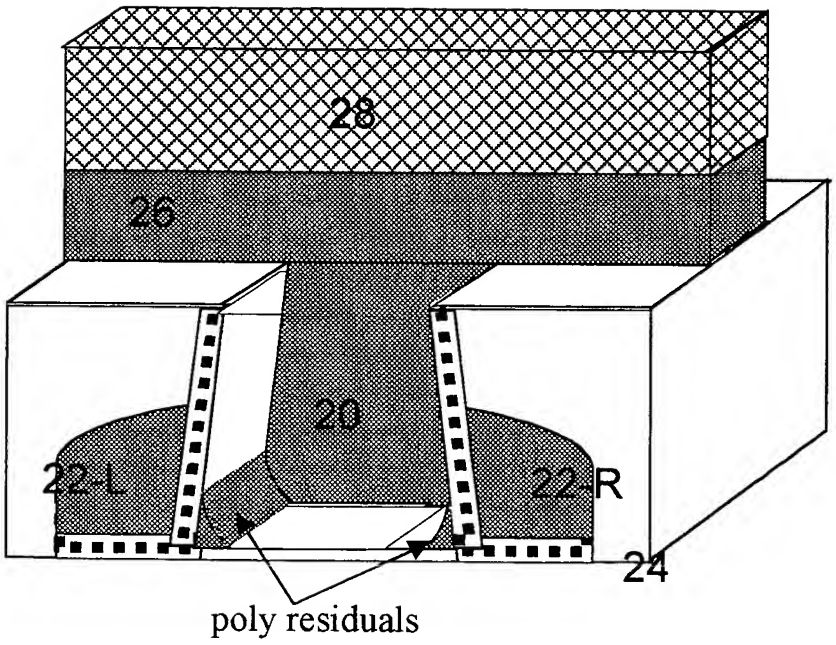


Fig.5B

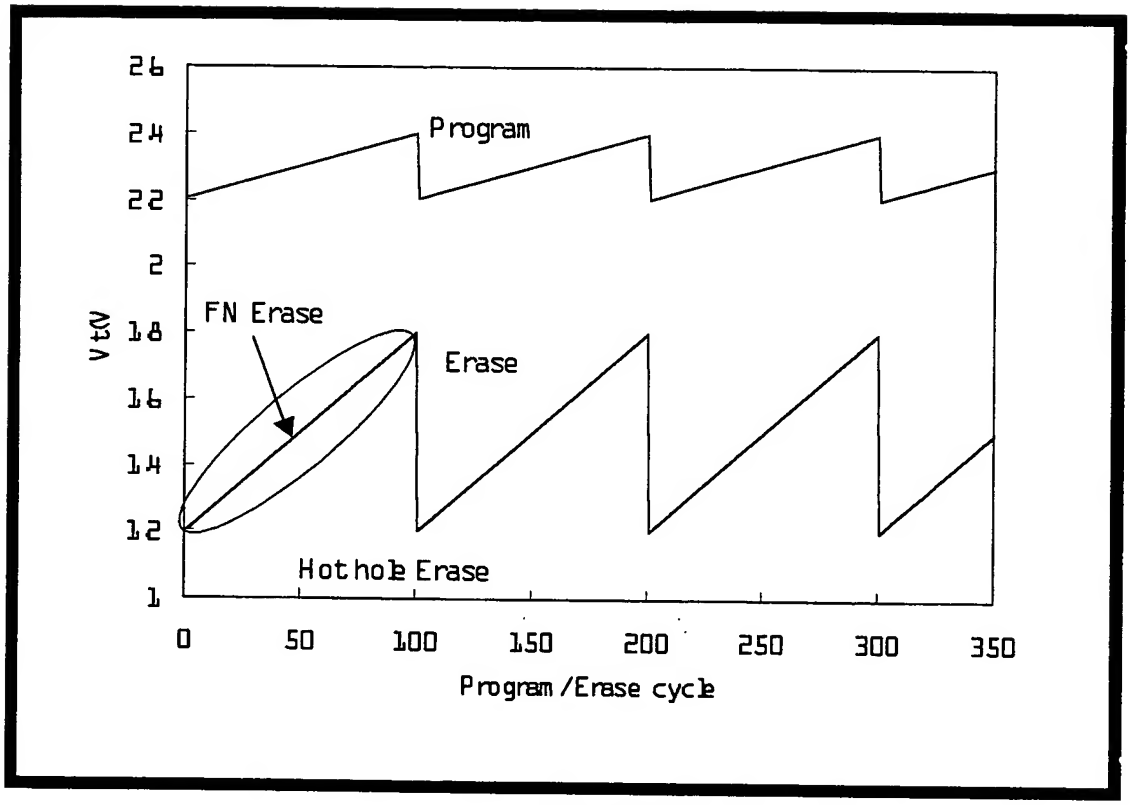

26
24
22
2
18
16
14
12
1
Vtw
Program
FN Erase
Erase
Hothole Erase
0
50
100
150
200
250
300
350
Program/Erase cycle

Fig.6

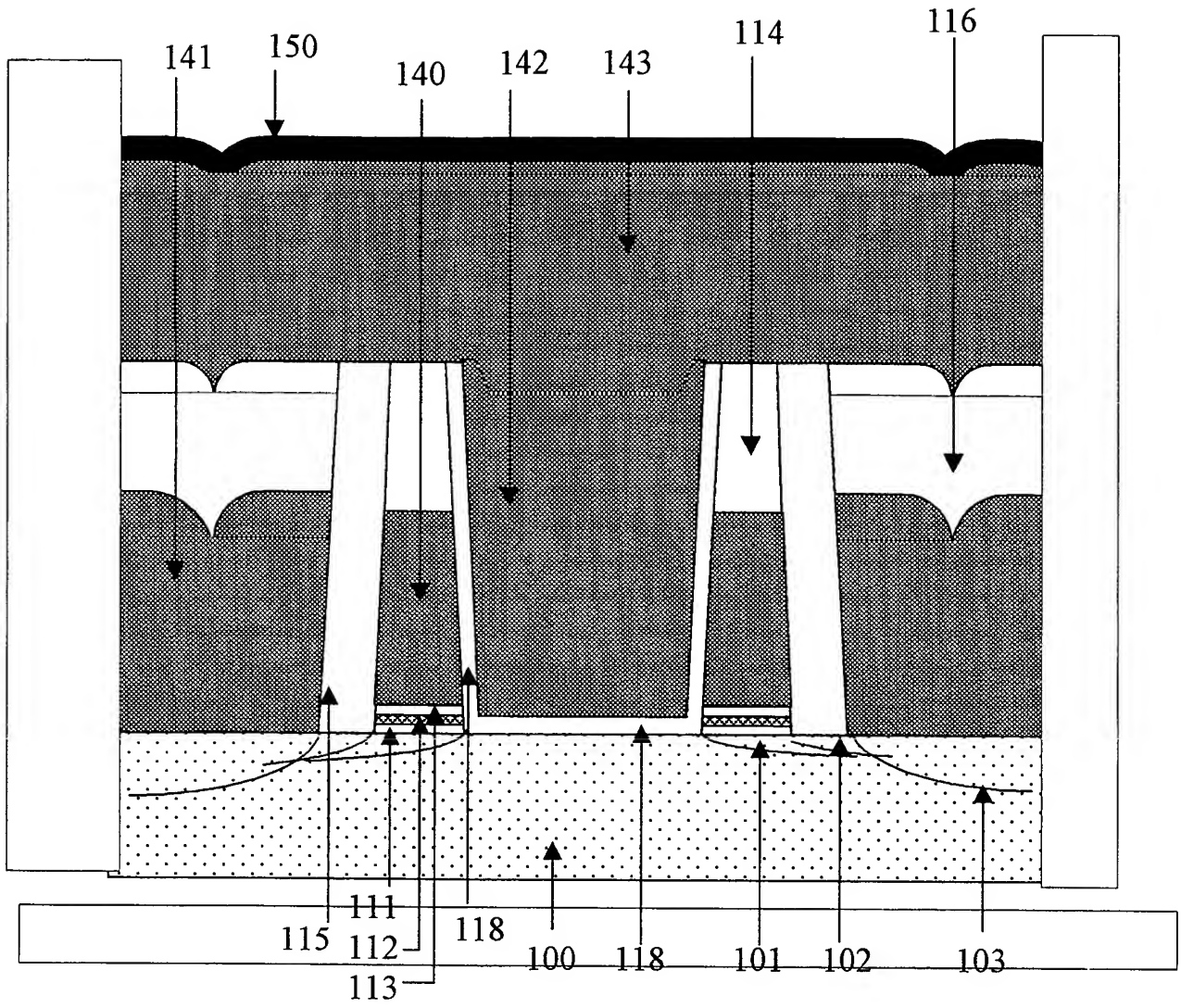


Fig.7

100 Substrate

101 Control Gate Channel

102 Memory LDD

103 Memory diffusion

111 ONO Bottom oxide

112 ONO Nitride

113 ONO Top oxide

114 CG Oxide Mask

115 Memory Spacer

116 Recess Oxide

117 CG-WG isolation

118 Word Gate Oxide

140 Control Gate Poly Si

141 Raised Diffusion Poly Si

142 Word gate

143 Word Line

150 Word Line Salicide

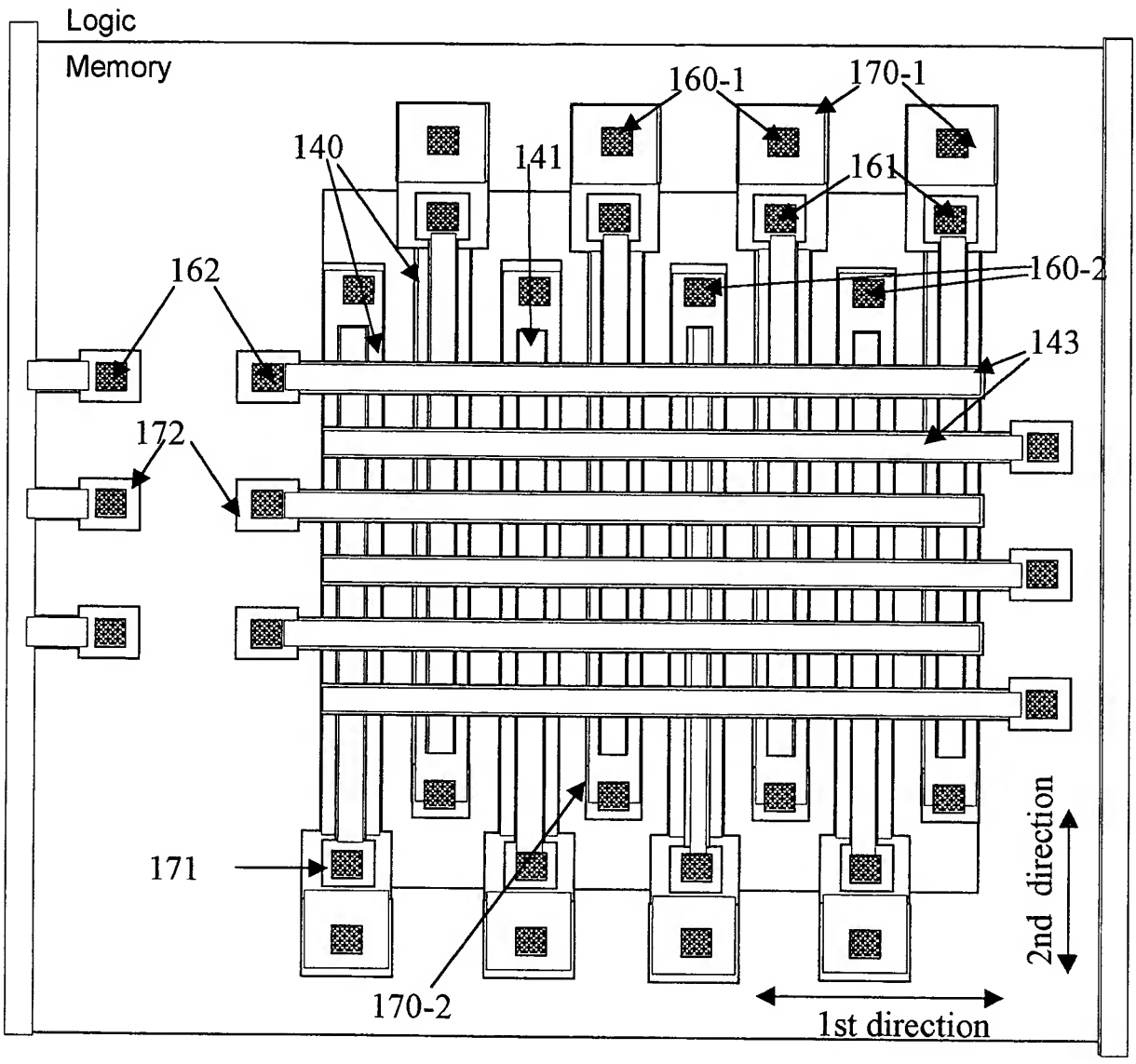


Fig.8

160-1Control Gate Contact type 1

160-2Control Gate Contact type 2

161 Bit line (Diffusion) Contact

162 Word line Contact

170-1Control Gate Contact type 1 Cover

170-2Control Gate Contact type 2 Cover

171 Bit line (Diffusion) Contact Cover

172 Word line Contact Cover

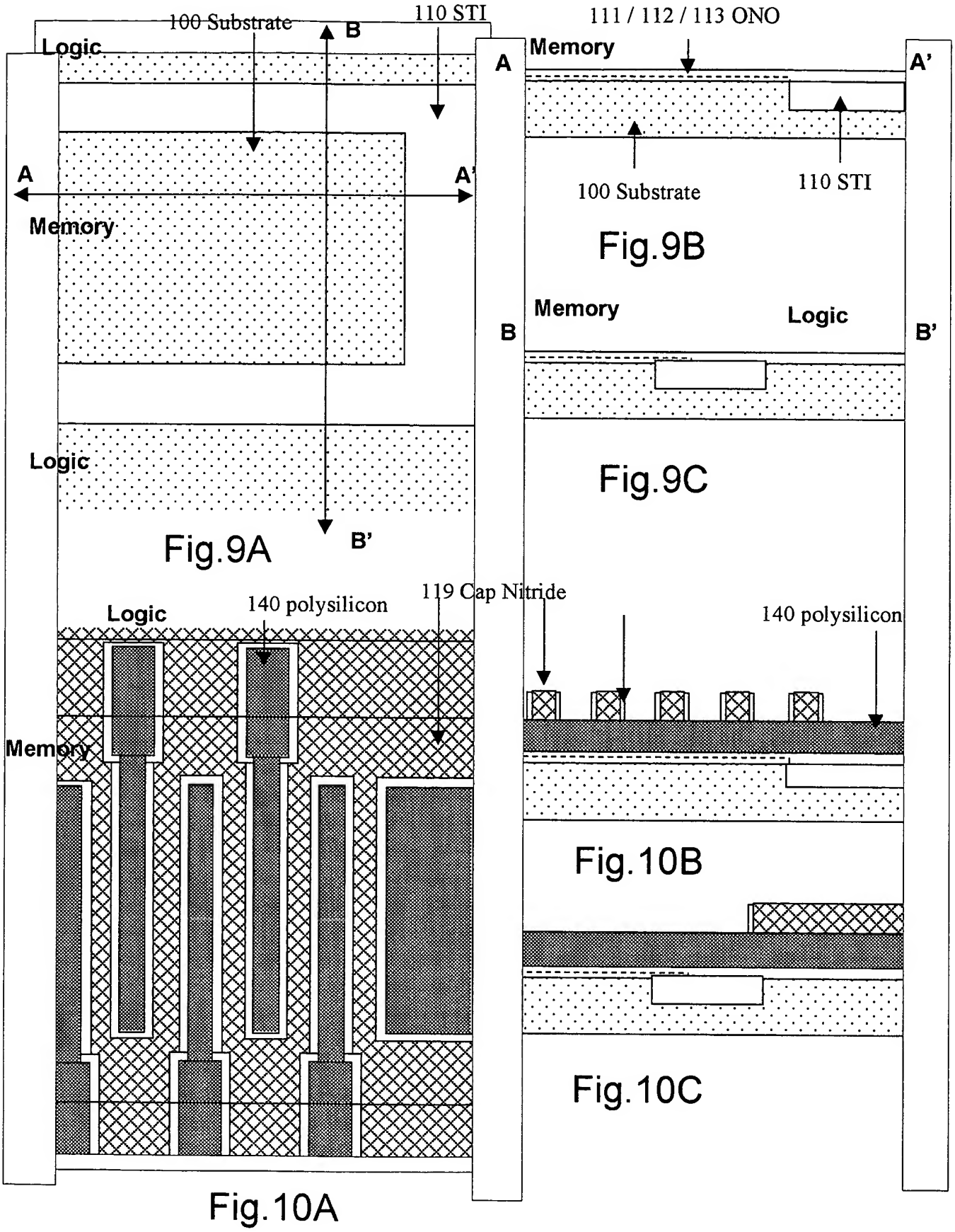


Fig.9A

Fig.9B

Fig.9C

Fig.10A

Fig.10B

Fig.10C

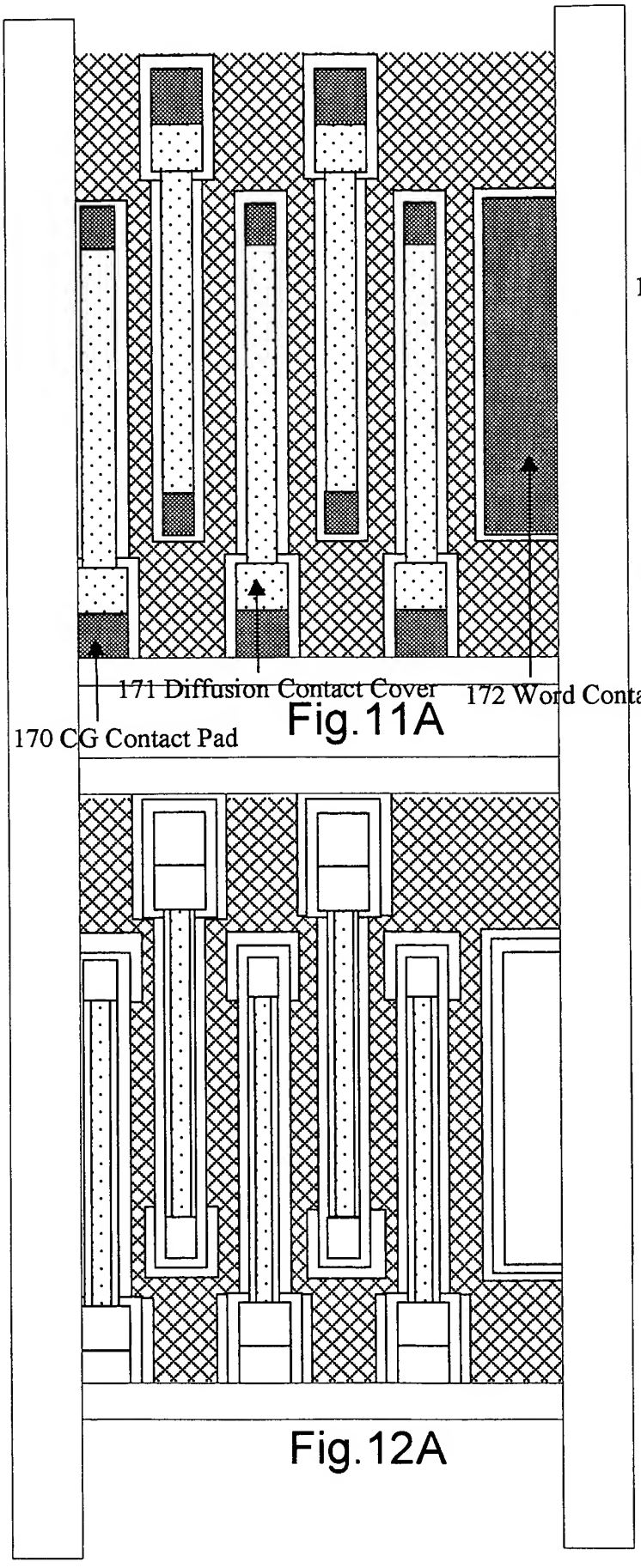


Fig.11A

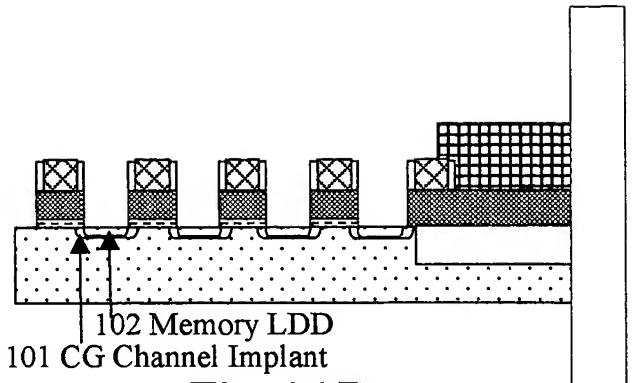


Fig.11B

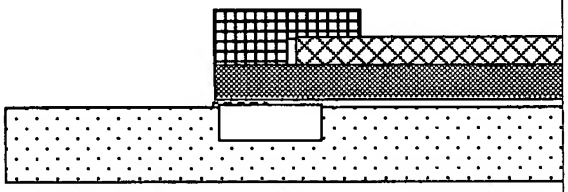


Fig.11C

Fig.12A

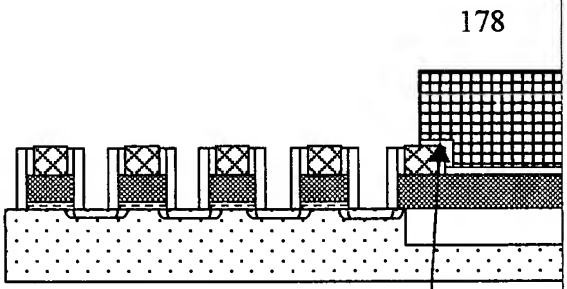


Fig.12B

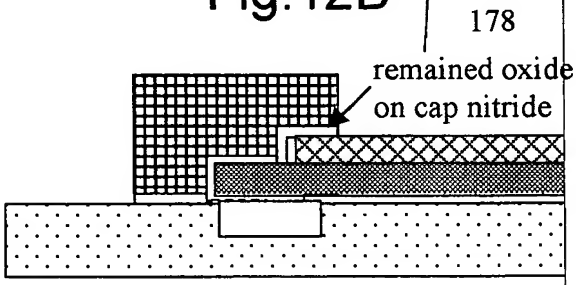


Fig.12C

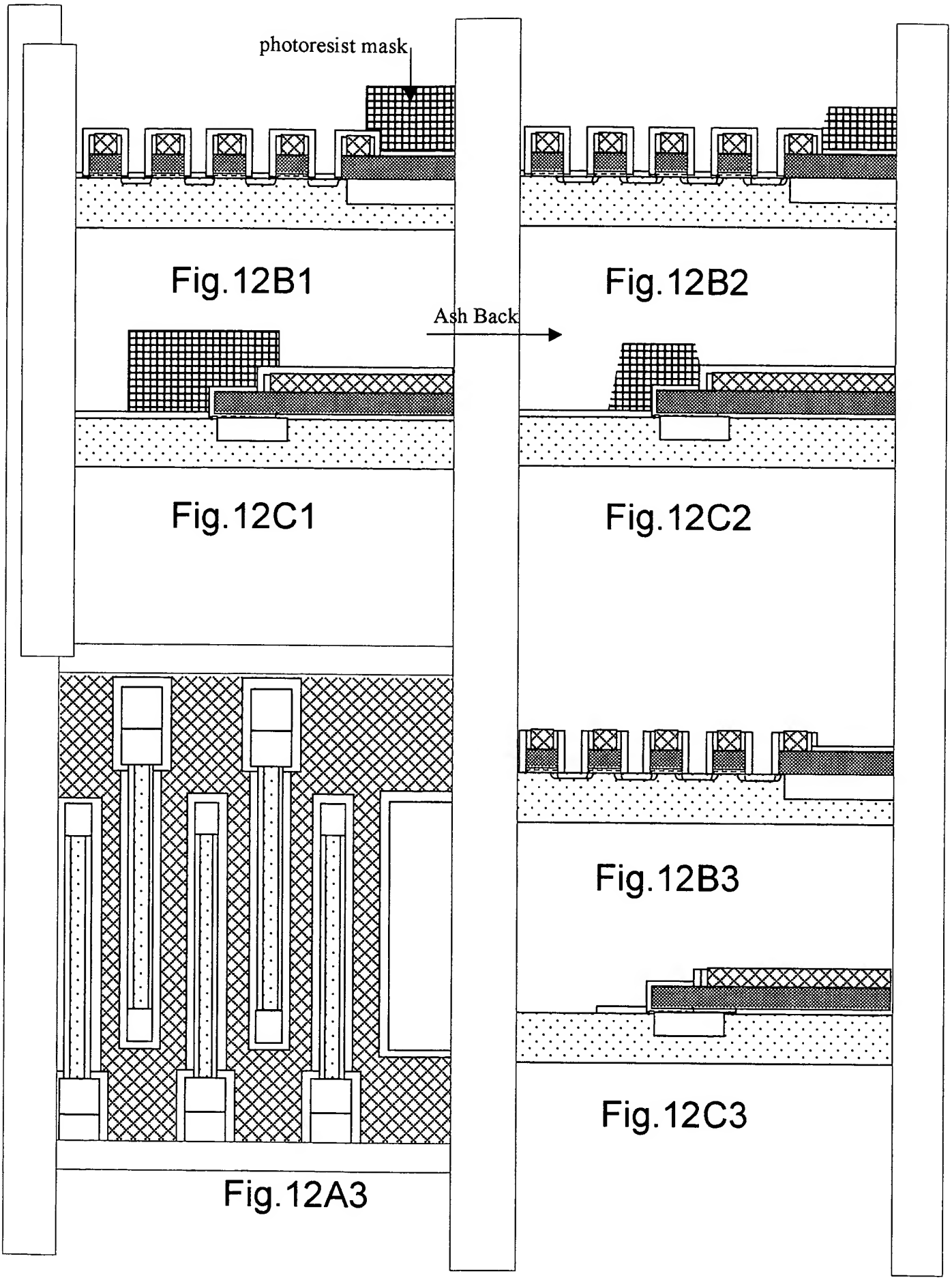


Fig.12B1

Fig.12B2

Fig.12C1

Fig.12C2

Fig.12B3

Fig.12C3

Fig.12A3

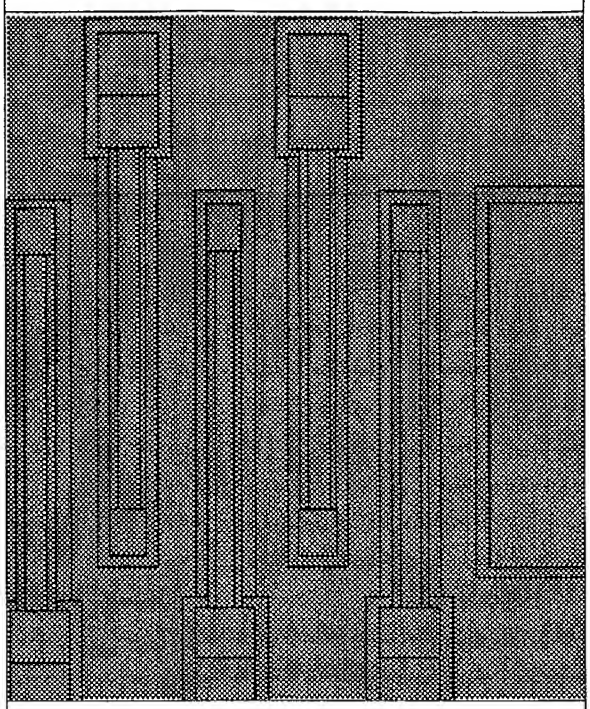


Fig.13A

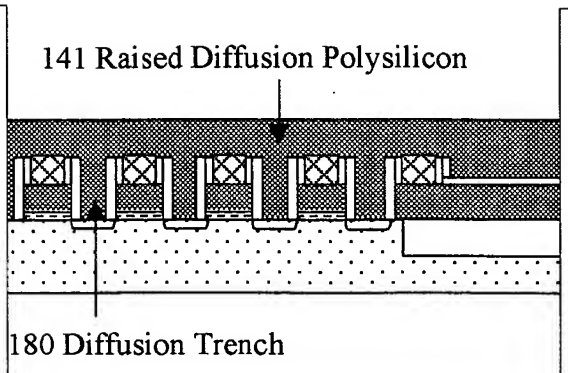


Fig.13B

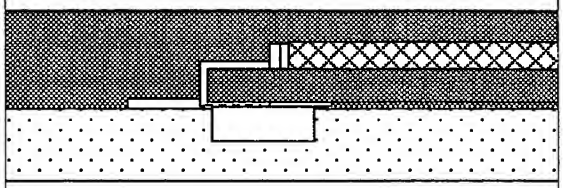


Fig.13C

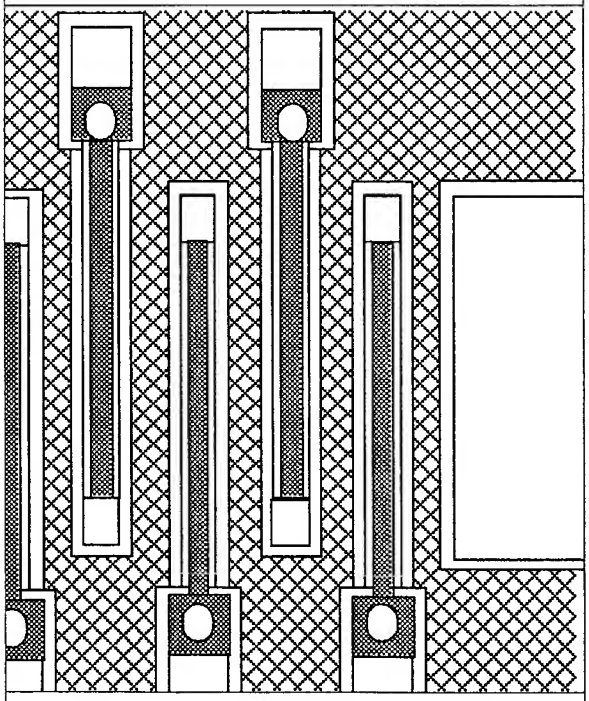


Fig.14A

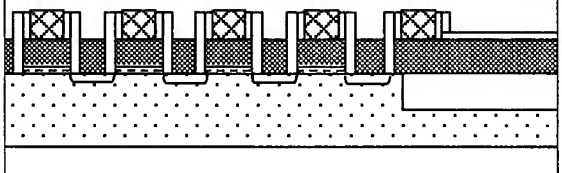


Fig.14B

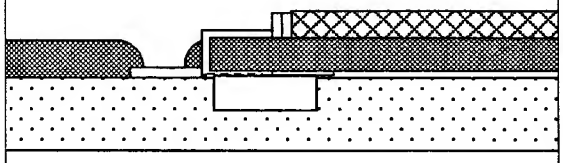


Fig.14C

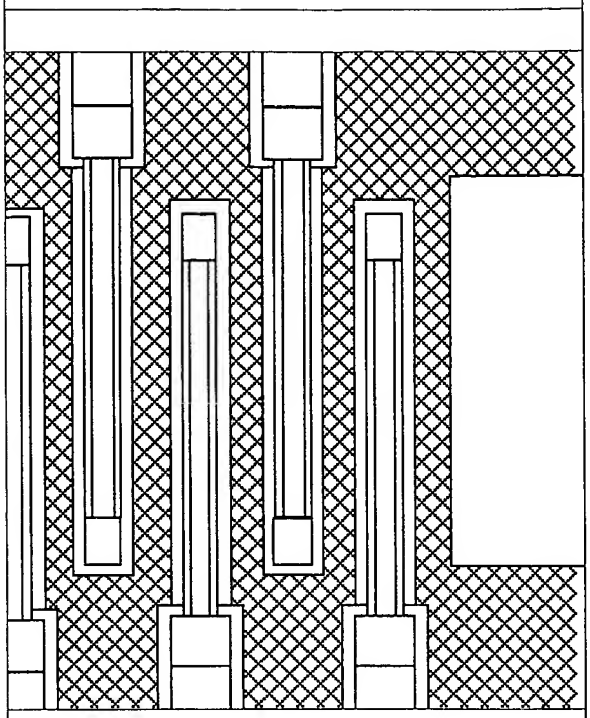


Fig.15A

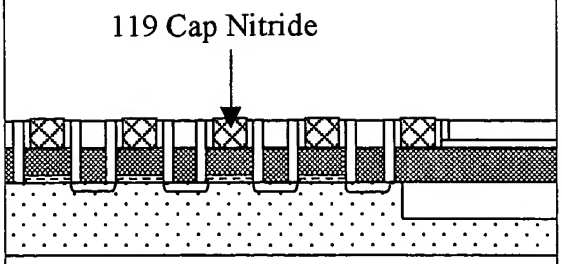


Fig.15B

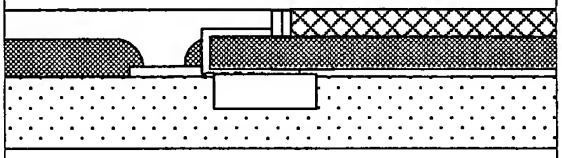


Fig.15C

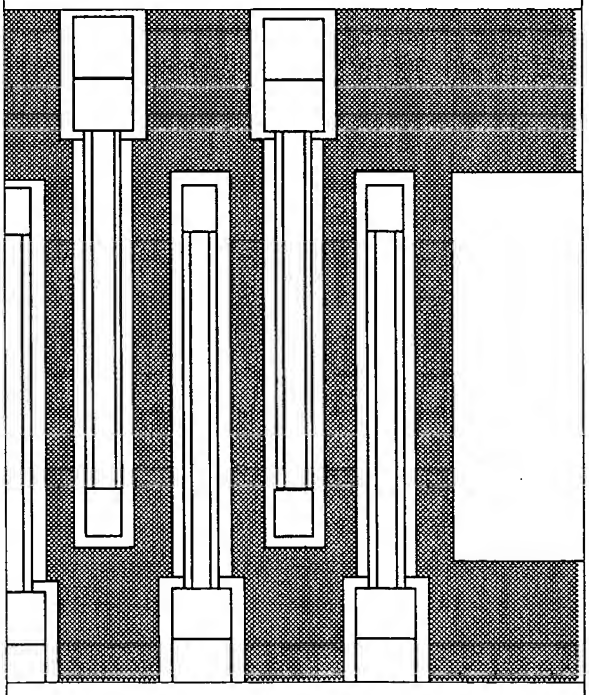


Fig.16A

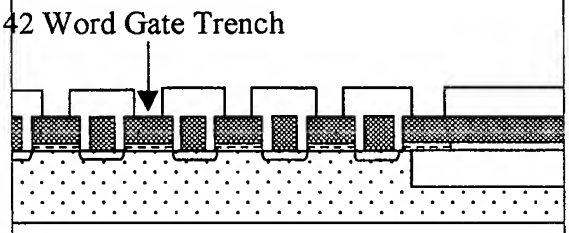


Fig.16B

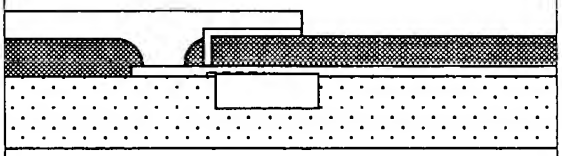


Fig.16C

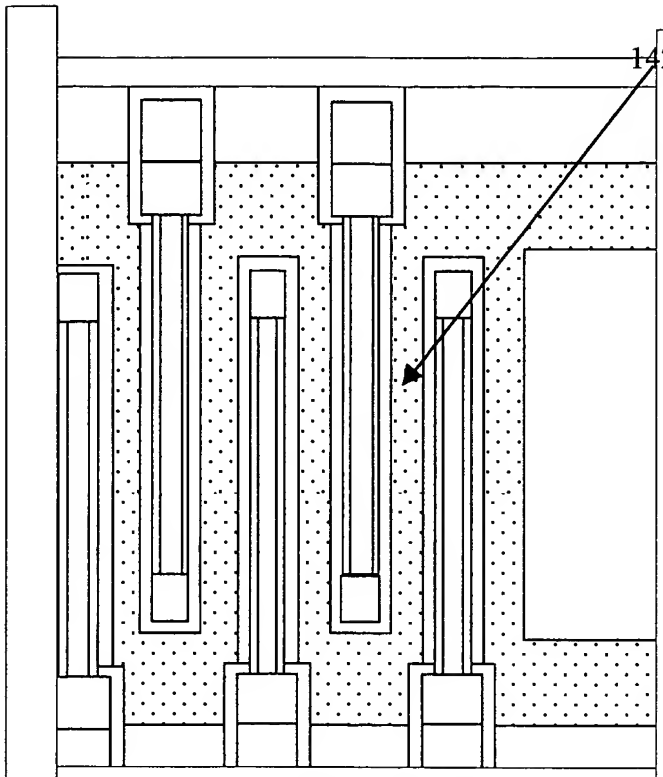


Fig.17A

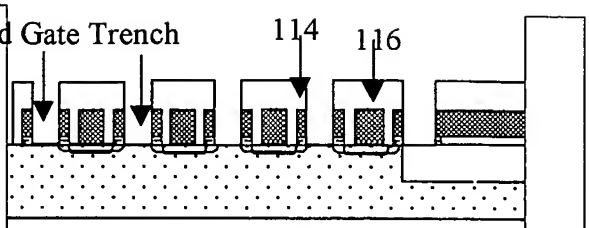


Fig.17B

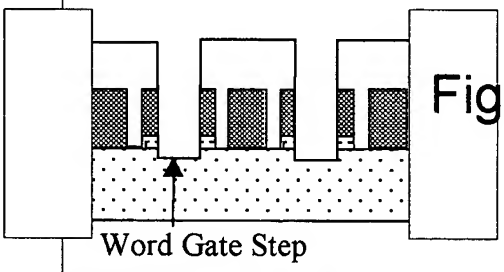


Fig.17B1

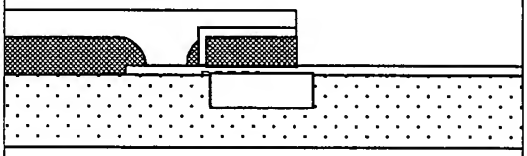


Fig.17C

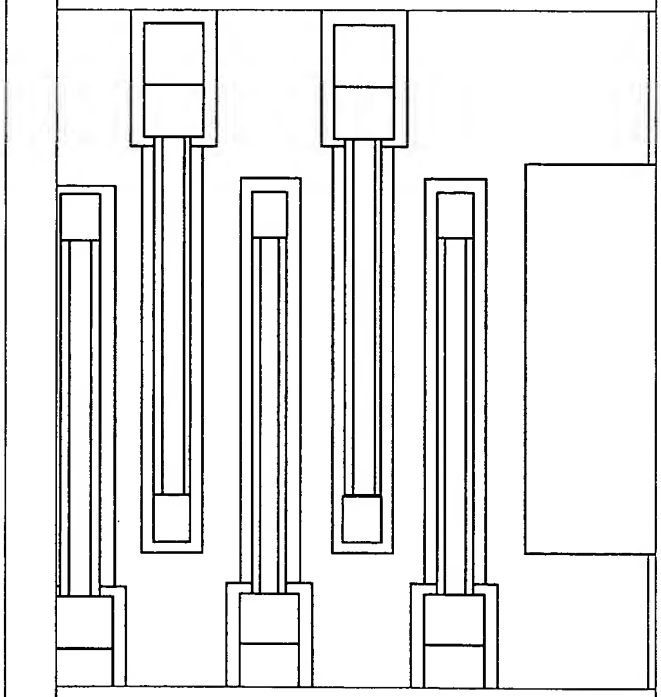


Fig.18A

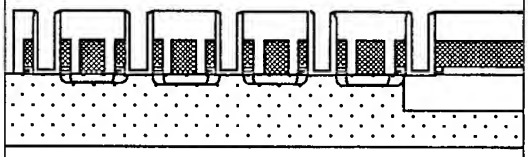


Fig.18B

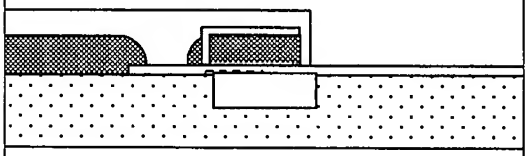


Fig.18C

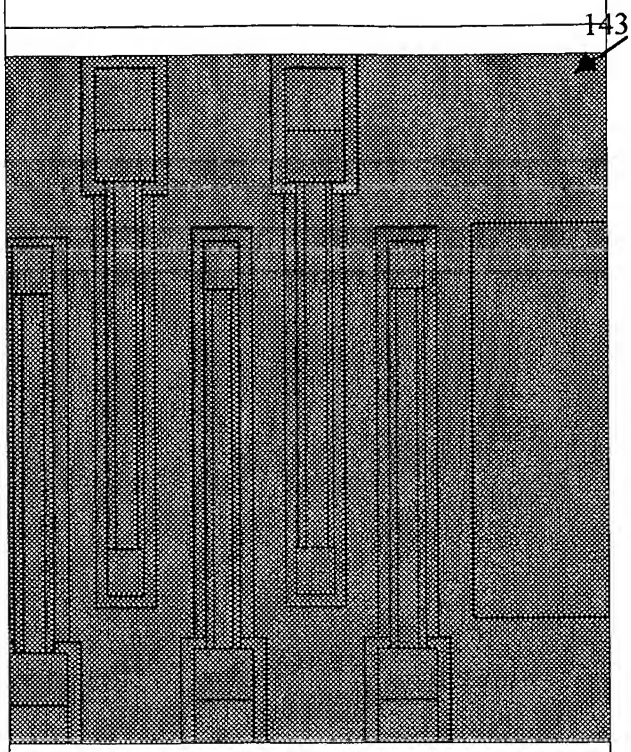


Fig.19A

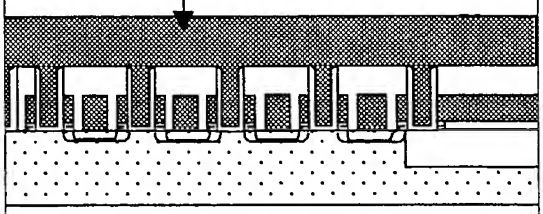


Fig.19B

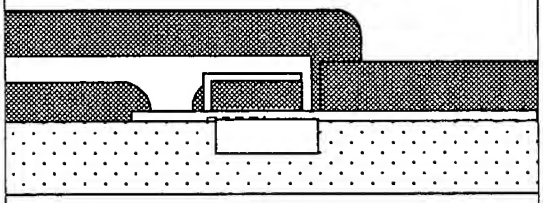


Fig.19C

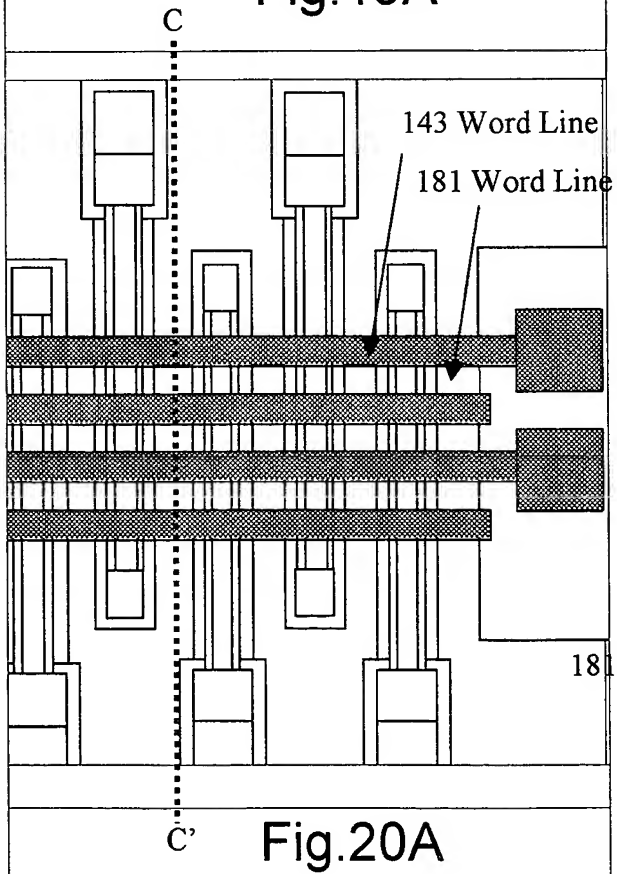


Fig.20A

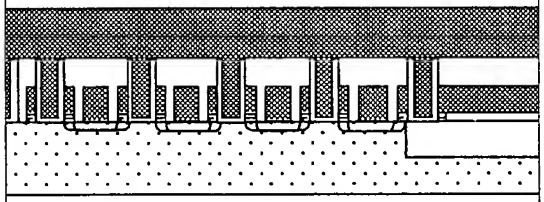


Fig.20B

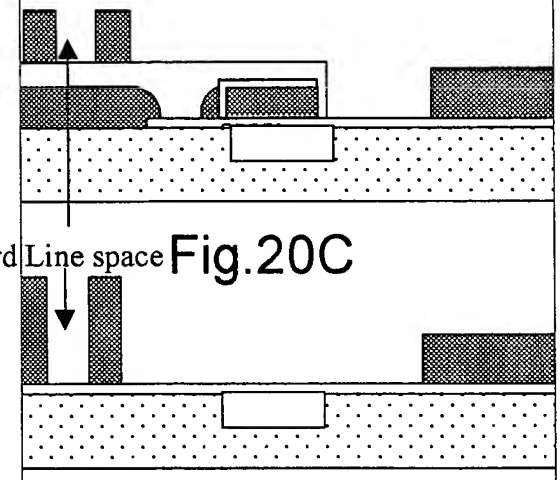


Fig.20C

Fig.20C1

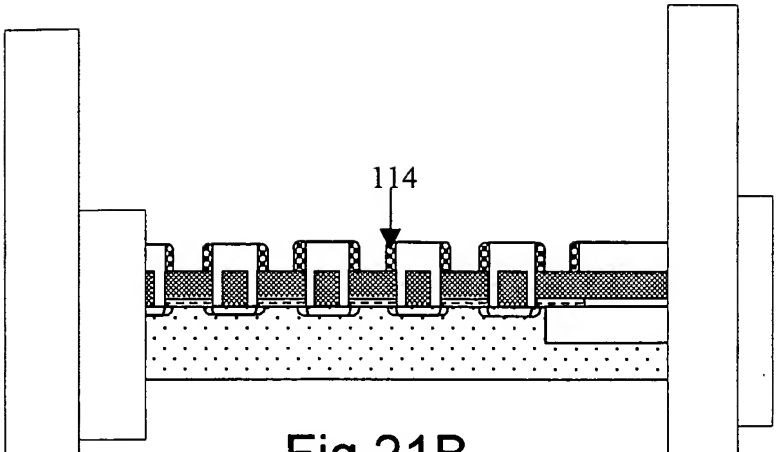


Fig.21B

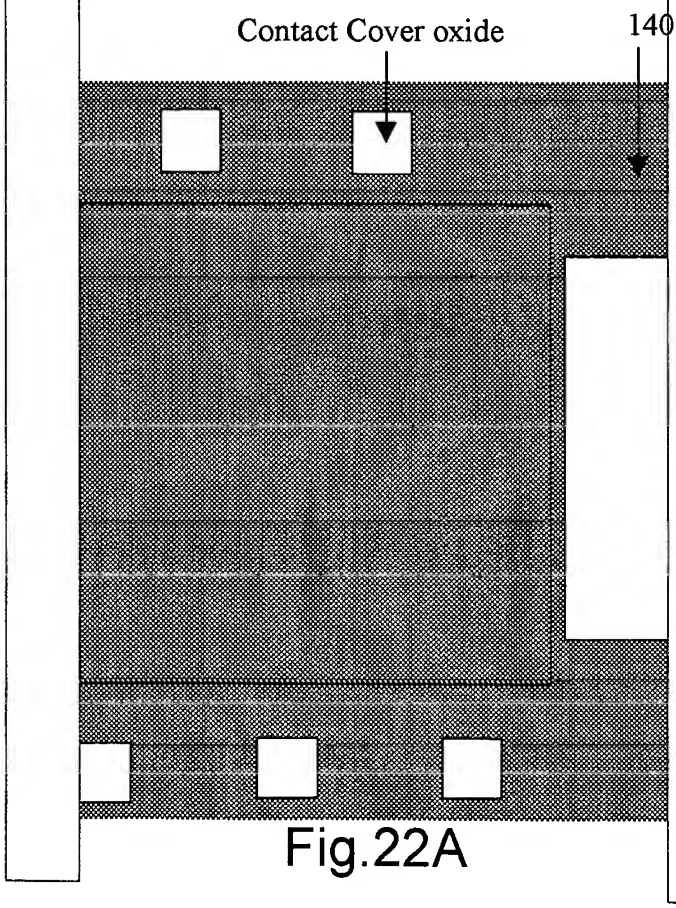


Fig.22A

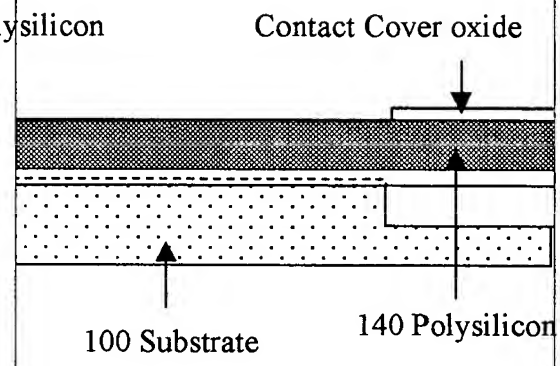


Fig.22B

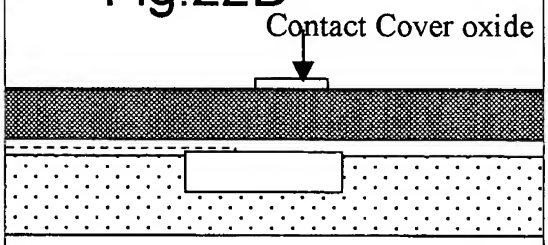


Fig.22C

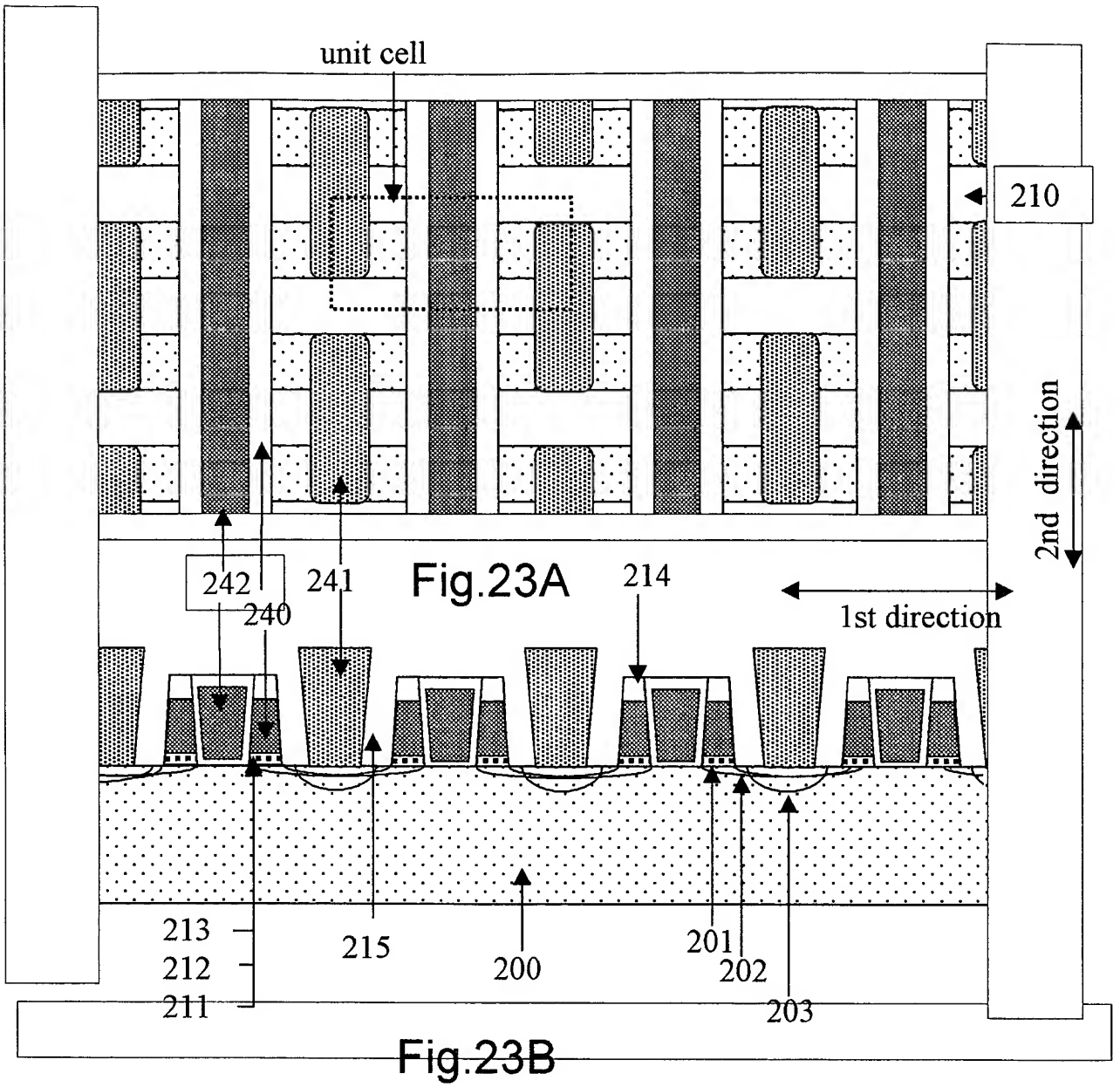


Fig.23A

Fig.23B

200 Substrate

201 Control Gate Channel

202 Memory LDD

203 Memory diffusion

211 ONO Bottom oxide

212 ONO Nitride

213 ONO Top oxide

214 CG Oxide Mask

215 Memory Spacer

216 CG-WG isolation

217 Word Gate Oxide

218 Word cap oxide

240 Control Gate Poly Si

241 Local wiring

242 Word gate/Line

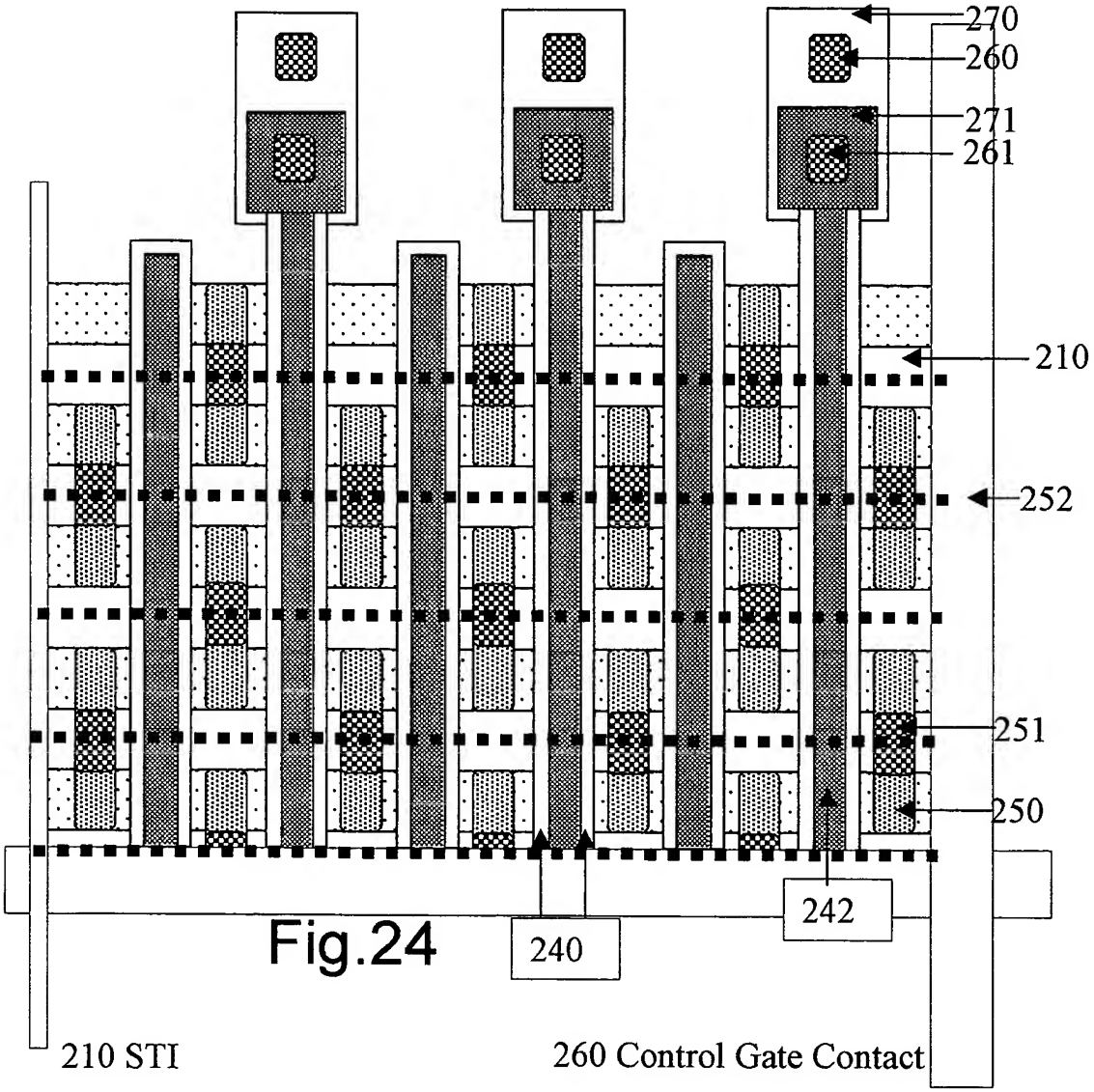


Fig.24

210 STI

240 Control Gate

242 Word Line

250 Local Wire (bit bridge)

251 Bit line Contact

252 Bit Line (1st Metal)

260 Control Gate Contact

261 Word Line Contact

270 Control Gate Contact Cover

271 Word line Contact Cover

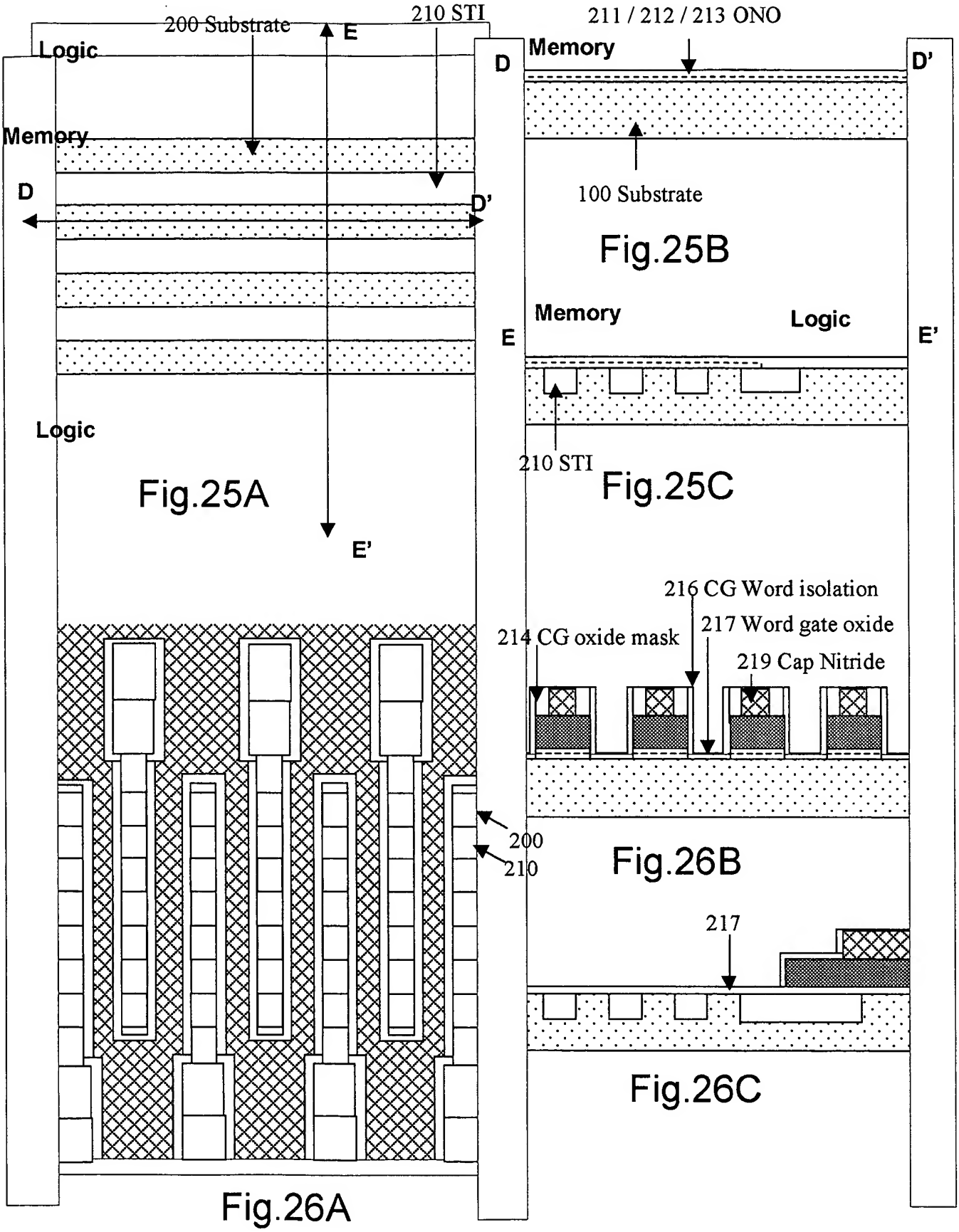


Fig.25A

Fig.25B

Fig.25C

Fig.26A

Fig.26B

Fig.26C

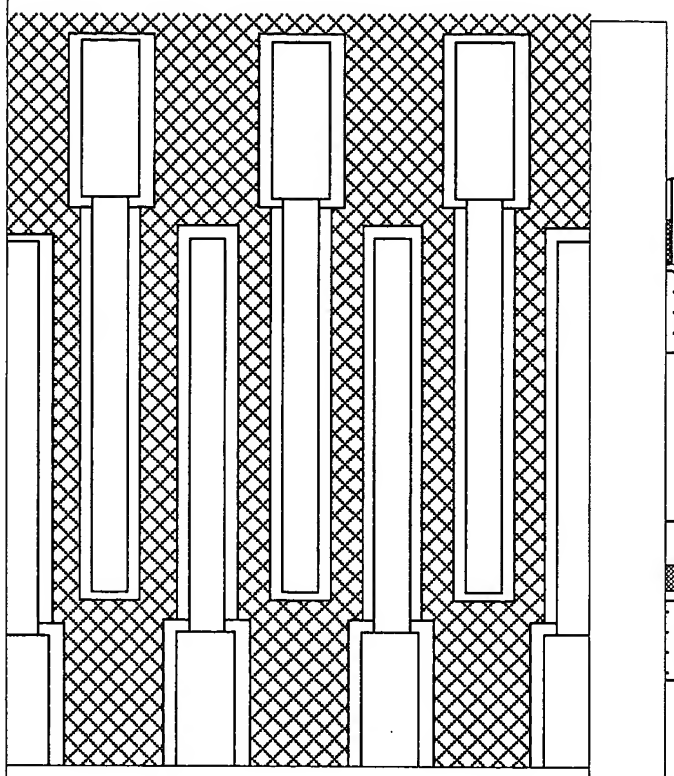


Fig.27A

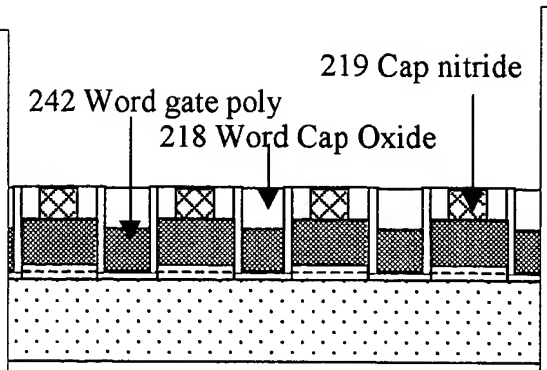


Fig.27B

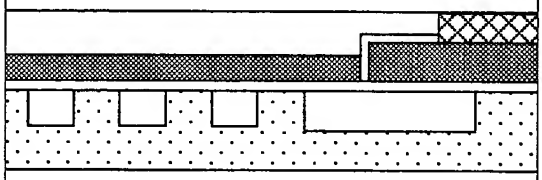


Fig.27C

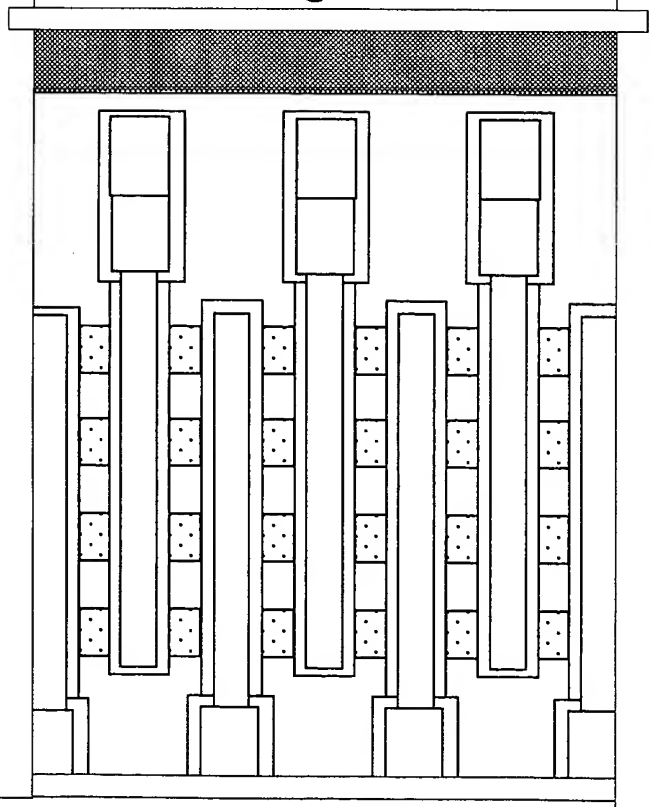


Fig.28A

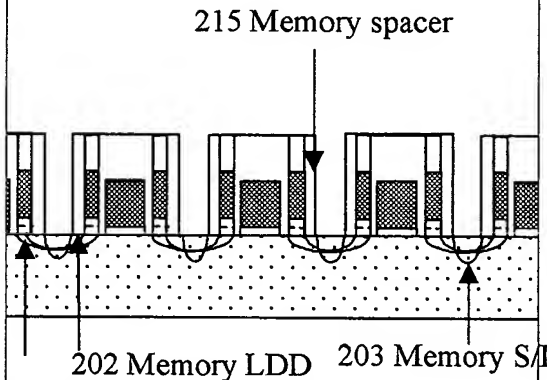


Fig.28B

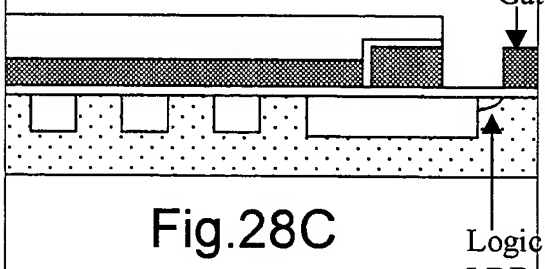
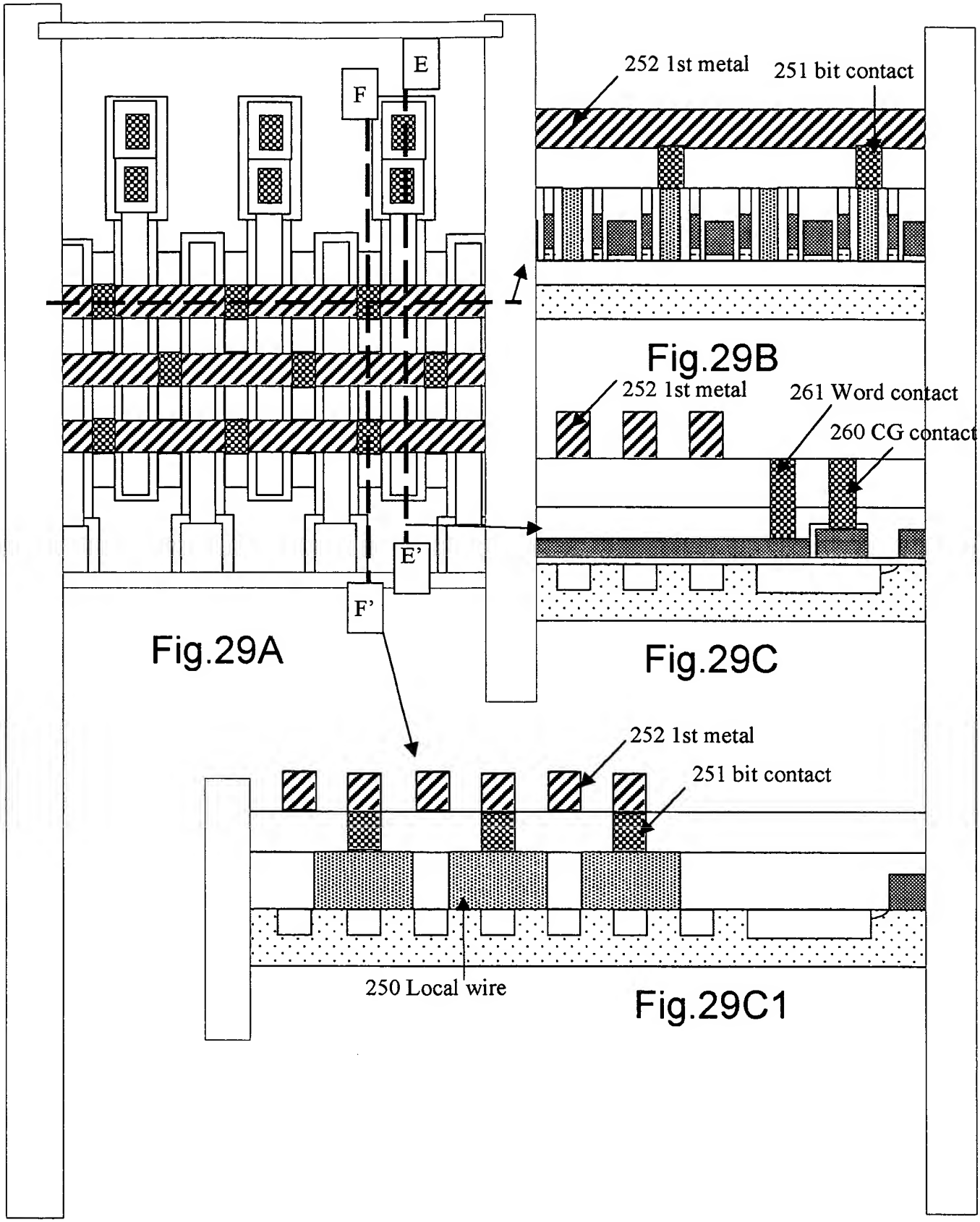


Fig.28C


E
F
E'
F'
1
252 1st metal
251 bit contact
Fig.29B
252 1st metal
261 Word contact
260 CG contact
Fig.29A
Fig.29C
252 1st metal
251 bit contact
250 Local wire
Fig.29C1

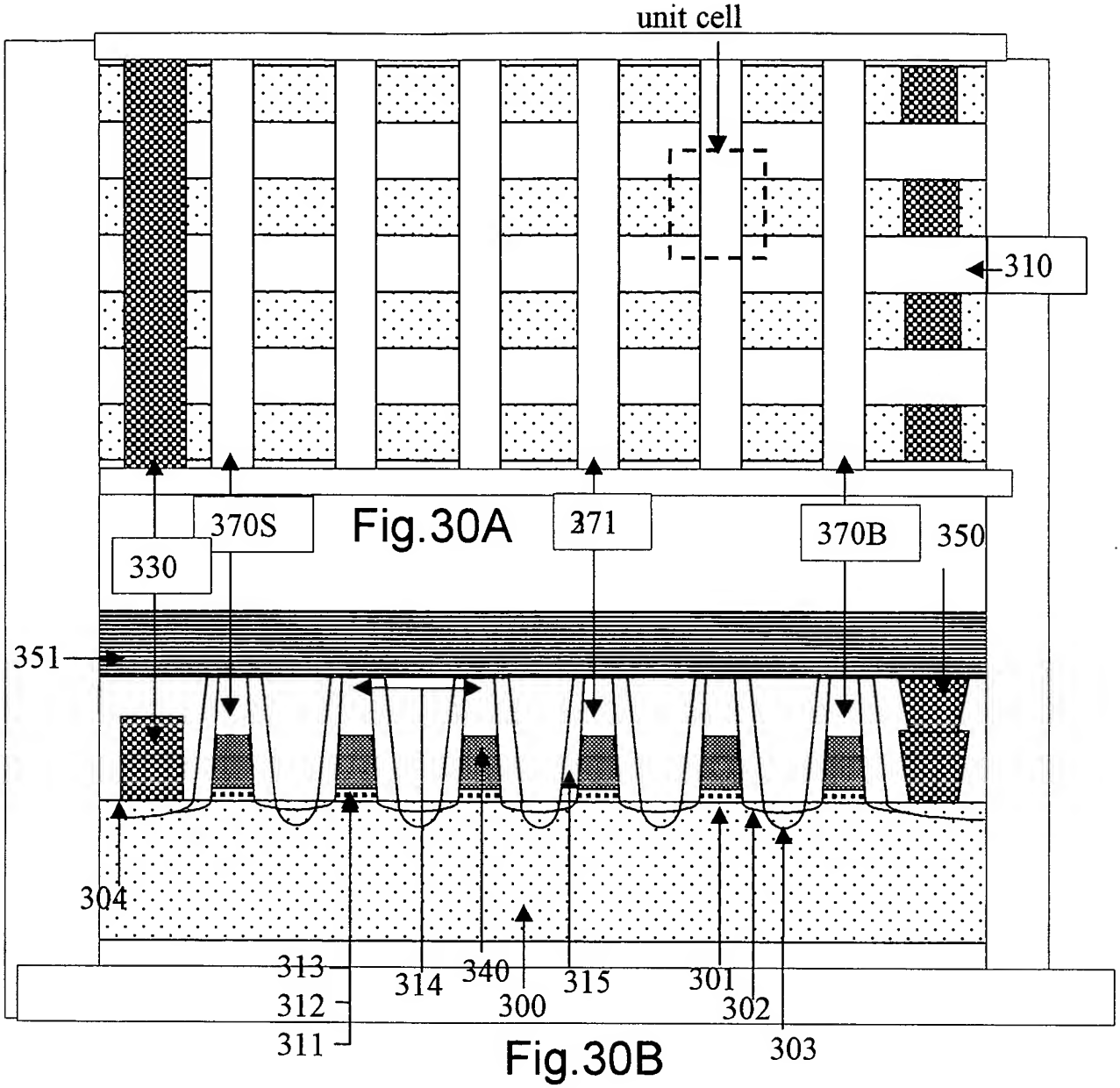


Fig.30A

Fig.30B

300 Substrate

301 Control Gate Channel

302 Memory LDD

303 Memory diffusion

304 Common Ground

310 STI

311 ONO Bottom oxide

312 ONO Nitride

313 ONO Top oxide

314 CG Oxide Mask

315 Memory Spacer

330 Local wiring

340 Control Gate Poly Si

350 Bit Contact

351 Bit Line (1st Metal)

370B Select Gate (Bit)

370S Select Gate (Source)

371 Control gate line

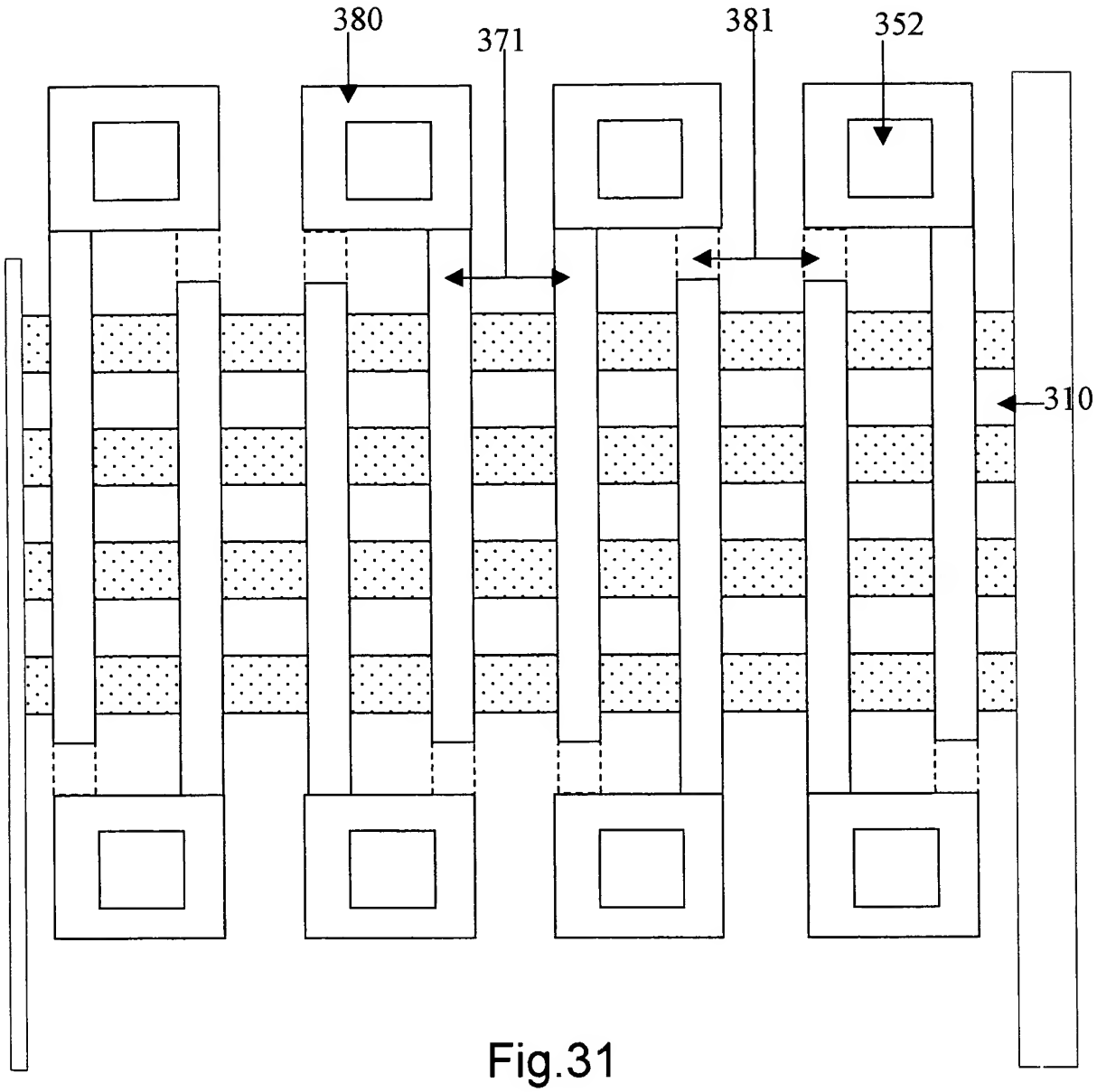


Fig.31

352 Control gate Contact

380 Control gate Contact Cover

381 Control gate Edge cut

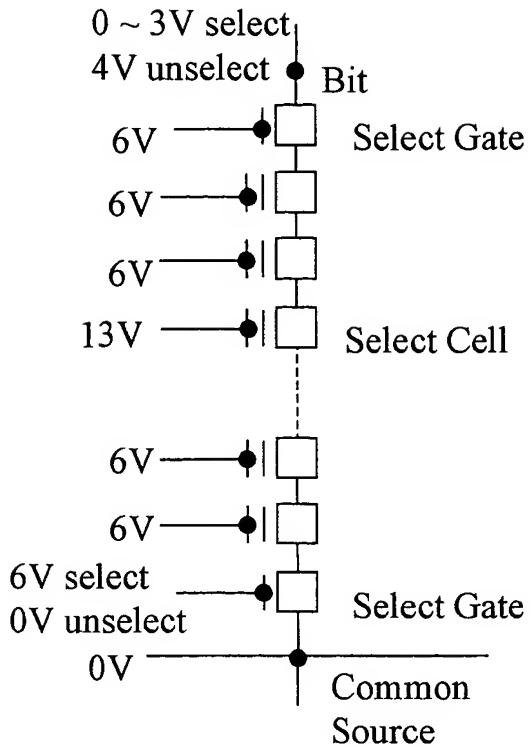


Fig.32A1

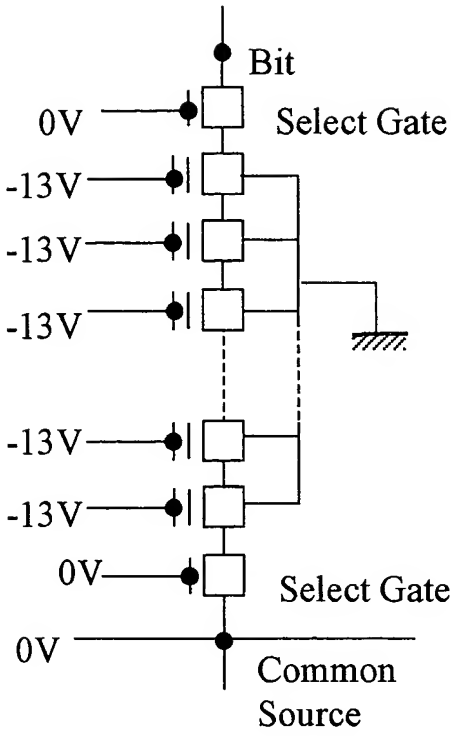


Fig.32A2

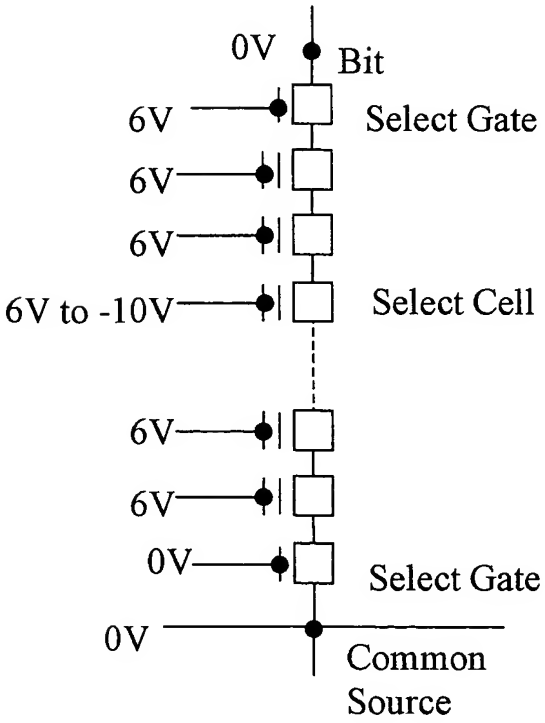


Fig.32B1

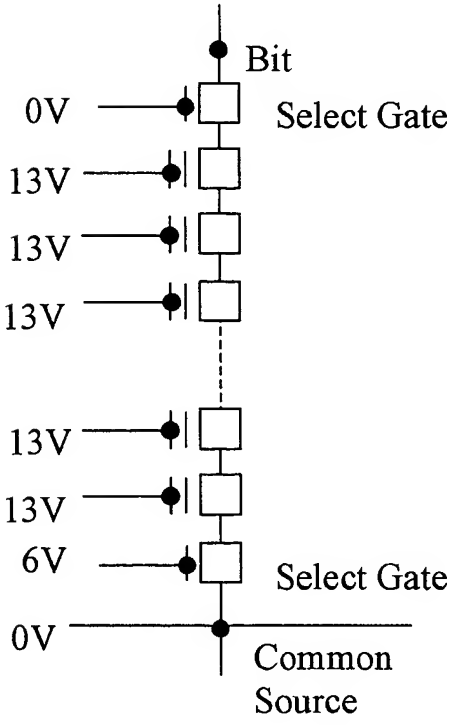


Fig.32B2

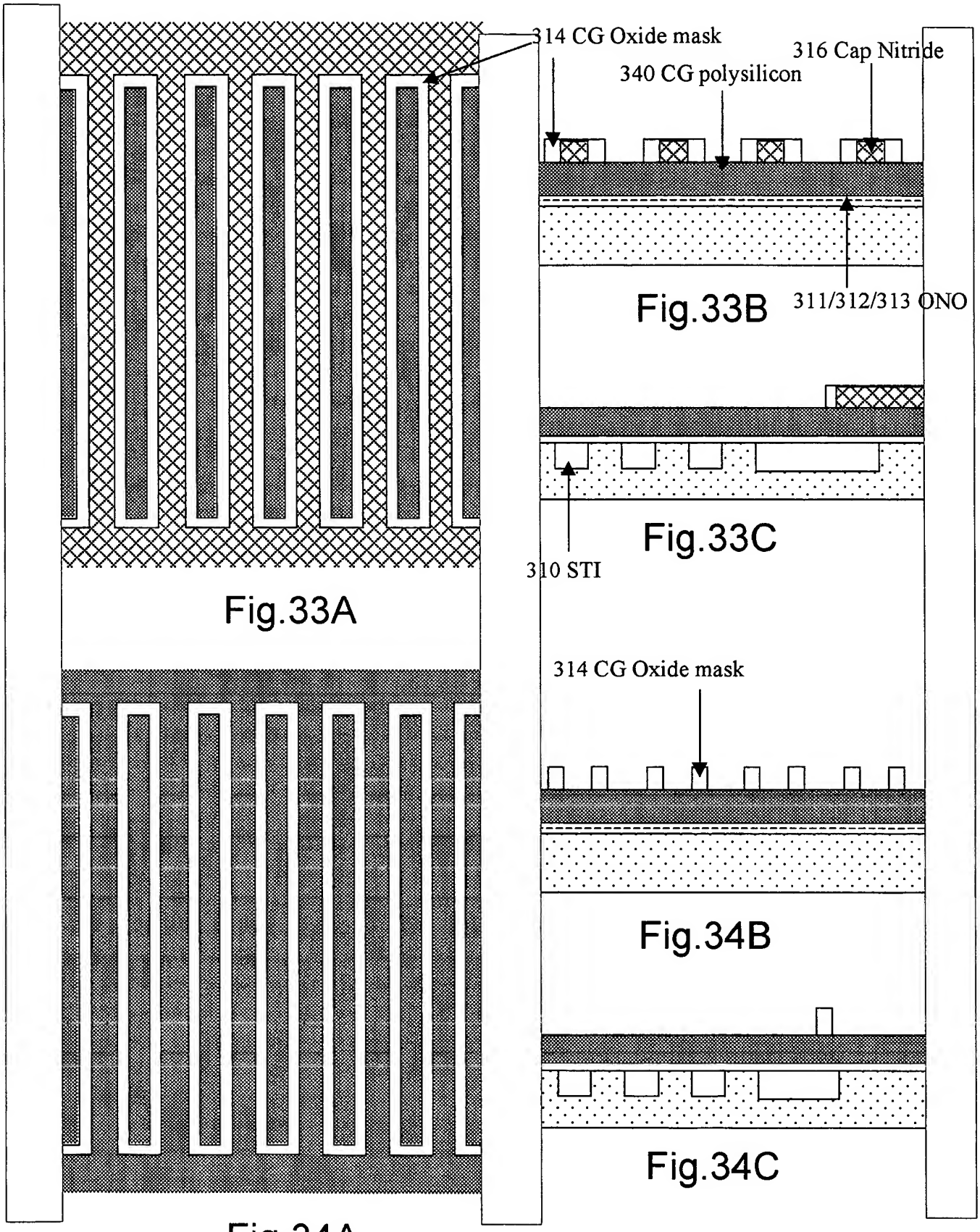


Fig.33A

Fig.33B

Fig.33C

Fig.34A

Fig.34B

Fig.34C

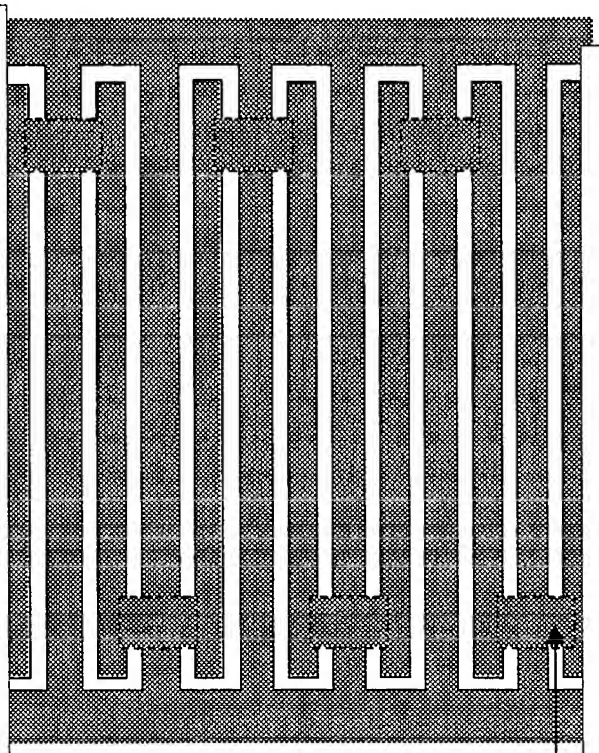


Fig.35A

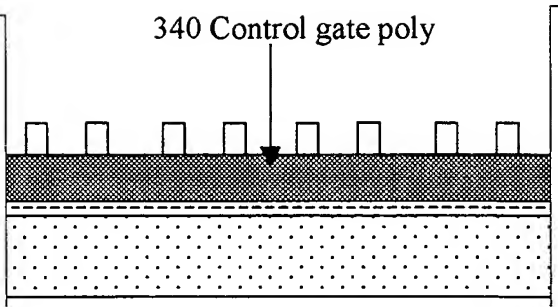


Fig.35B

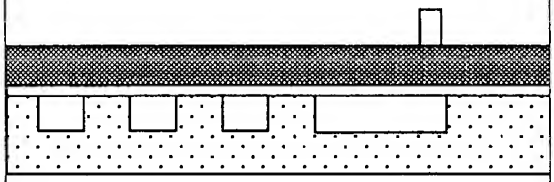


Fig.35C

381 CG edge cut

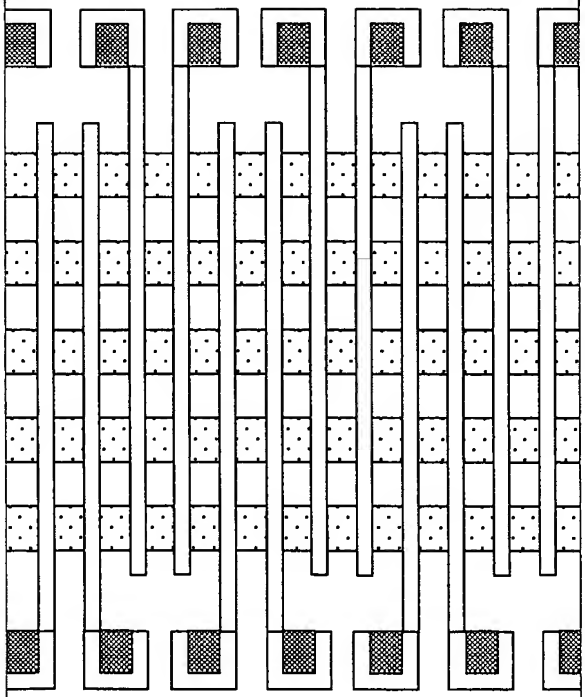


Fig.36A

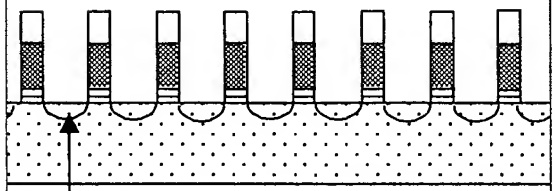


Fig.36B

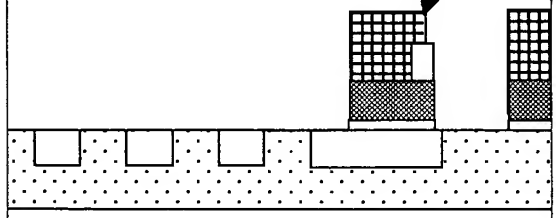


Fig.36C

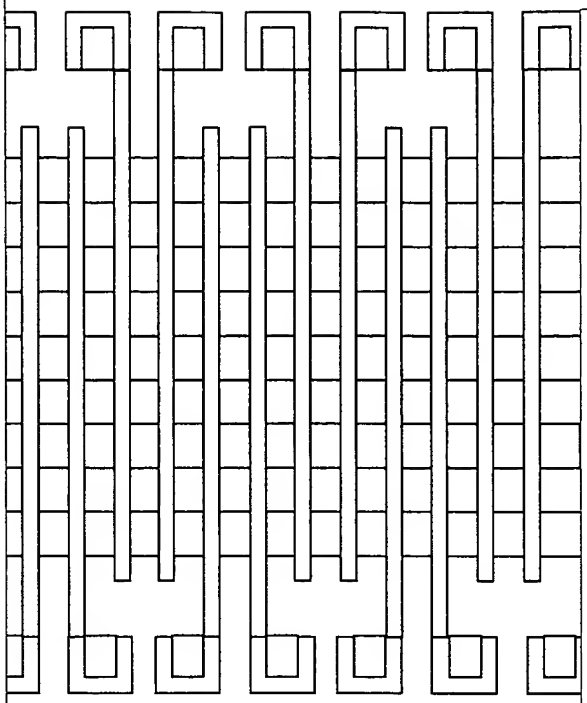


Fig.37A

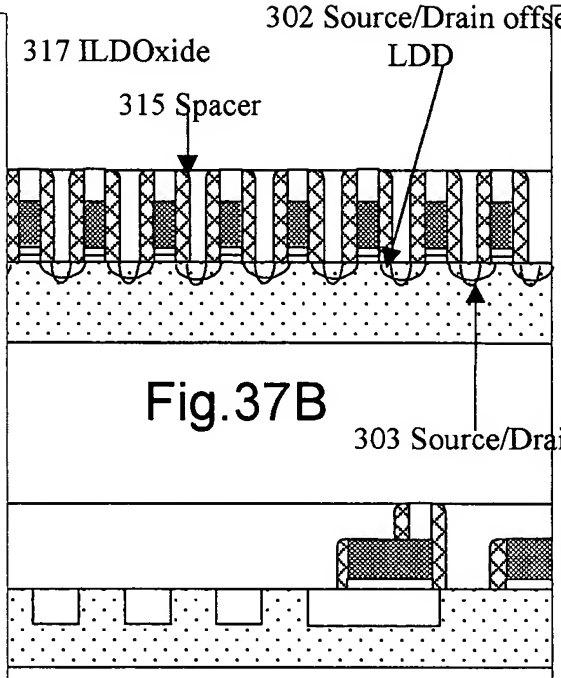


Fig.37B

Fig.37C

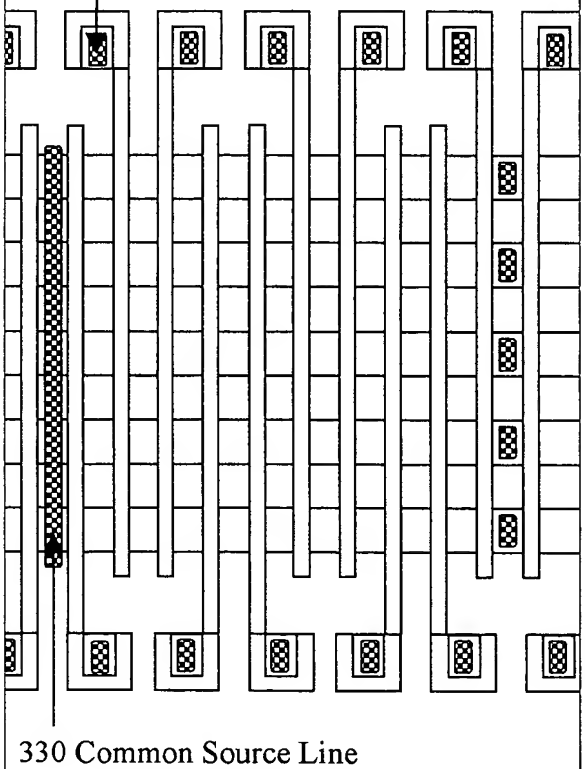


Fig.38A

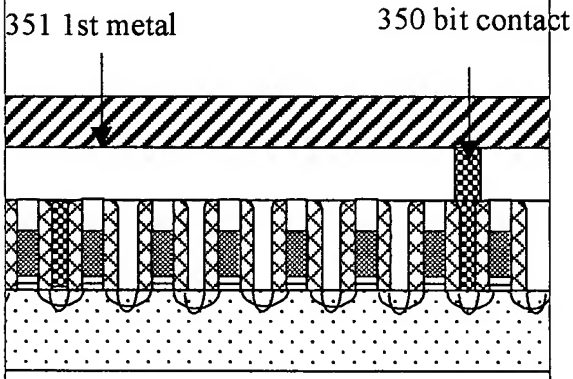


Fig.38B

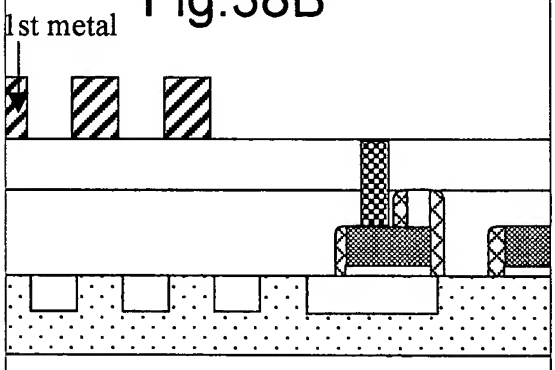


Fig.38C

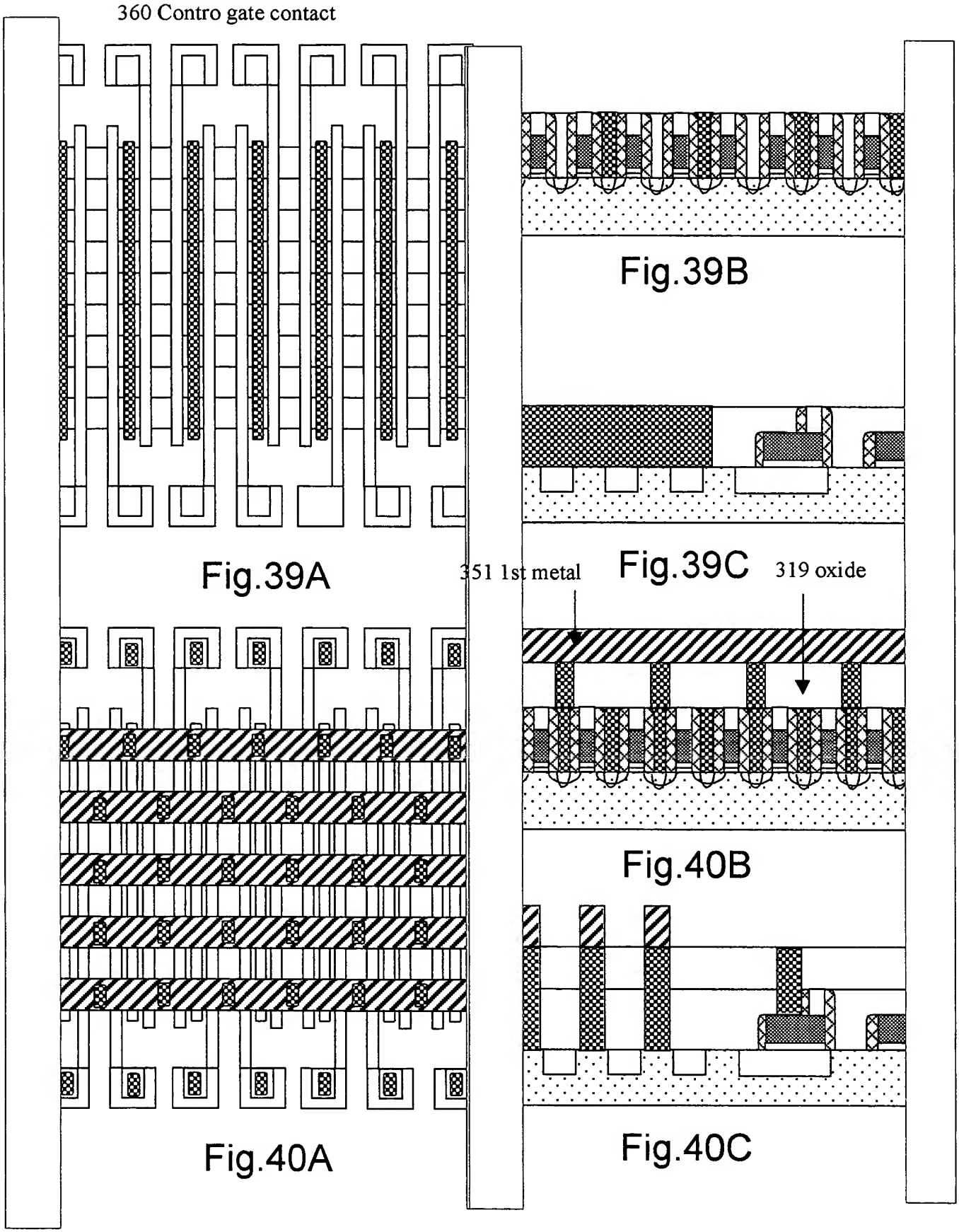


Fig.39A

Fig.39B

Fig.39C

351 1st metal

319 oxide

Fig.40A

Fig.40B

Fig.40C

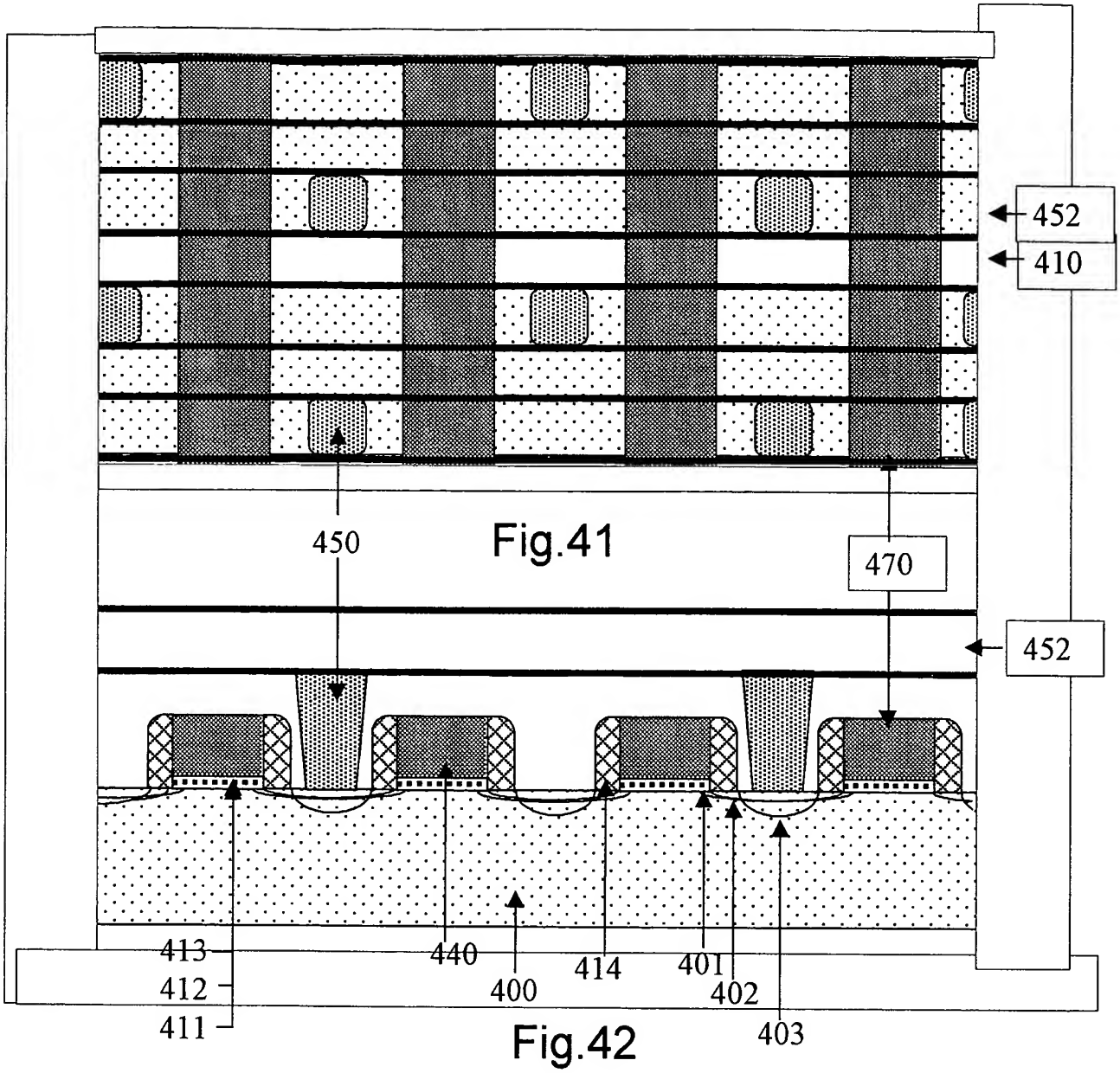


Fig.41

Fig.42

400 Substrate

401 Memory Halo

402 Memory LDD

403 Memory diffusion

410 STI

411 ONO Bottom oxide

412 ONO Nitride

413 ONO Top oxide

415 Memory Spacer

440 Memory gate Si

450 Local wire (bit bridge)

451 Bit contact

452 Bit Line (1sr metal)

470 Word Line

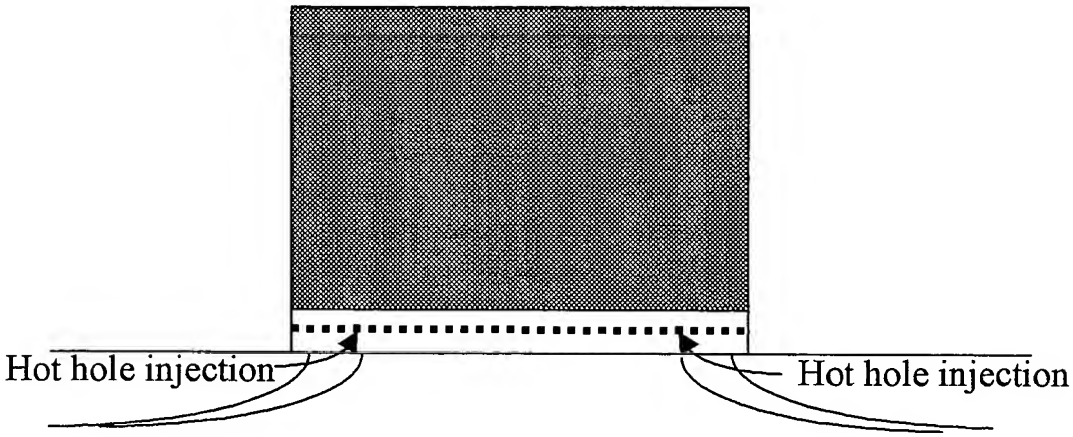

Hot hole injection
Hot hole injection

Fig.43

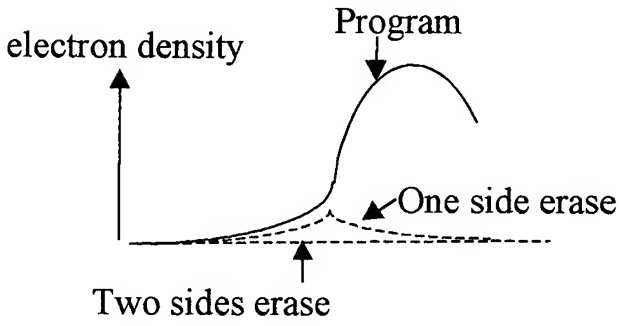

electron density
Program
One side erase
Two sides erase

Fig.44